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High Resolution Direct Digitization and Optical Telemetry of Shipboard Antenna Signals

by

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FORWARD

This research examines an optical architecture for directly digitizing shipboard antenna signals with high resolution. Transmission of the bits over fiber to the receivers below deck is also investigated. This research was performed by the faculty and students in the Optical Electronics Laboratory under the direction of Dr. Phillip E. Pace. The project is funded by the Space and Naval Warfare Systems Command PMW-178. This interim report covers the time period October 1993 to September 1994. Much thanks goes to Capt. Ristorcelli and Mr. Gerald Peake of PMW-178 for their guidance and support. The authors also wish to thank LT Rick Walley, LT Craig Crowe, and LT Hiromishi Yamakochi from the Optical Electronics Laboratory at the Naval Postgraduate School. Much thanks also goes to Mr. Rick Patterson of NRad and Mr. Jim Allen who typeset the entire manuscript.

ABSTRACT

This report describes the past year's research efforts (October 1993–September 1994) in the design, development and construction of an optical processing system to directly digitize and transport shipboard antenna signals to below deck. The electro-optical guidedwave analog-to-digital converter directly digitizes the antenna signals and is based on preprocessing the signals with a symmetrical number system (SNS) to achieve both an 8-bit design and a 14-bit design. The status of the hardware construction is described (8-bit expected completion — March 1995, 14-bit expected completion — July 1995). Using time division multiplexing (TDM) techniques, an optical digital link transports the bits over fiber to the receiver below deck.

1 INTRODUCTION

1.1 Optical Telemetry of Shipboard Antenna Signals

Shipboard antenna signals (e.g., direction-finding signals) are first transported below deck and then down converted to intermediate frequencies (IFs) before the analog-to-digital conversion can be performed and the information extracted. The bulky coax cables used to carry the signals from the antenna to below deck have a number of drawbacks including the susceptibility to electromagnetic interference (EMI). The down-conversion process requires RF mixers which ultimately limit the dynamic range.

Lightwave technology offers a number of advantages in relaying the antenna signals below deck. Figure 1 shows the architecture currently being researched. Among these advantages are the lighter weight and smaller volume of optical cable compared to shielded coax, the immunity from electromagnetic interference, and the availability of wide-bandwidth, high-speed channels [1]. Analog-to-digital converters that utilize optical technology also offer a number of advantages in the conversion of wideband analog signals into the digital domain. Using integrated optical processors to directly digitize the wideband signals at the antenna, the need to down-convert the signals to IF is eliminated. The large dynamic range available also removes the need for notch filters and automatic gain control circuits that can effectively hide important signals of interest.

1.2 Integrated Optical Guided-Wave Signal Processing

There are many situations in which the transmission and manipulation of optical power using optical dielectric waveguides can lead to major gains in performance

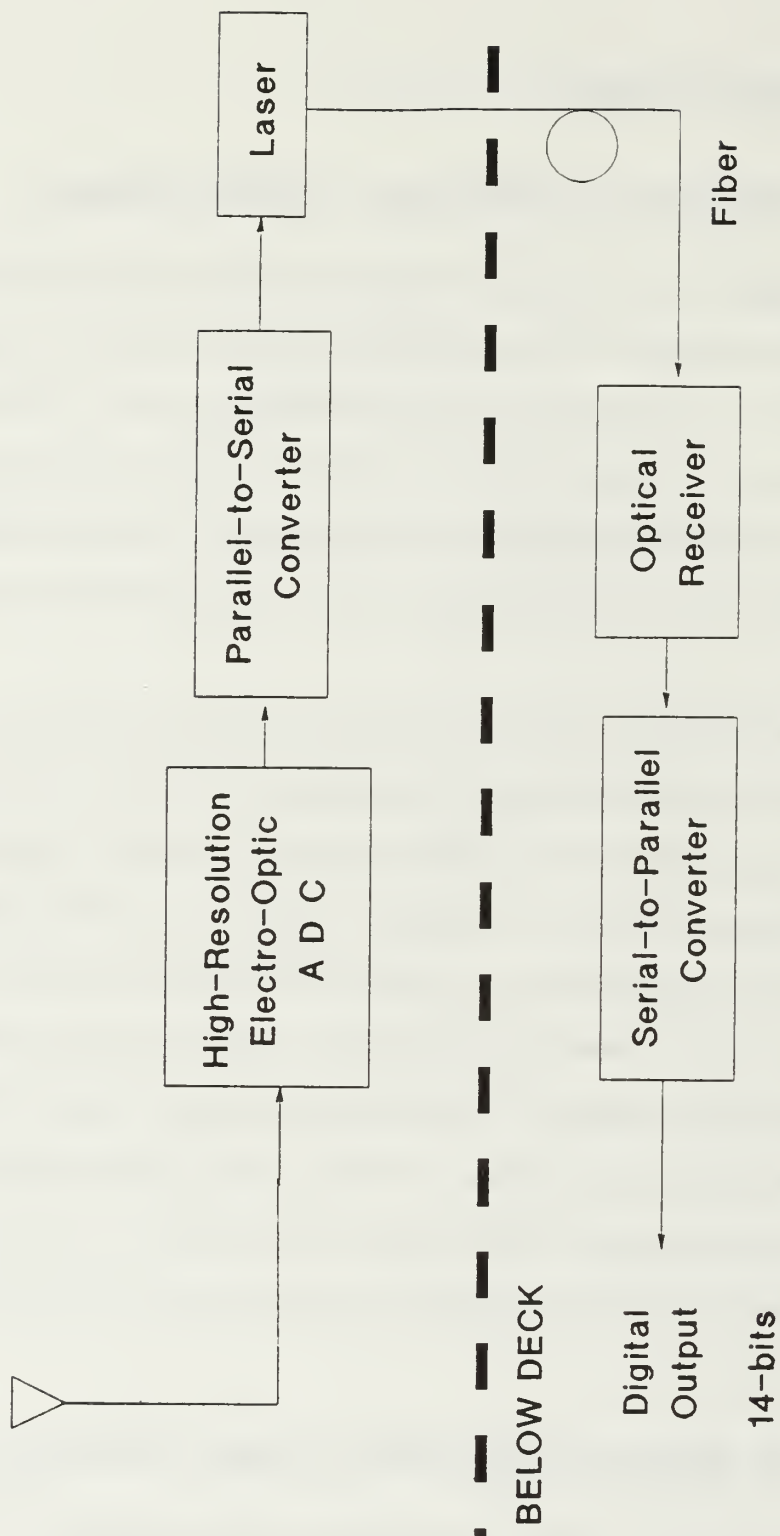


Figure 1: Optical processing architecture for telemetry of shipboard antenna signals.

compared with the approach of using bulk optics or electronic processors. Integrated optical architectures are small in size, have small power requirements, and, unlike electronic processors, EMI does not pose a problem to their performance. The large information capacity and the capability for massive parallel processing enables architectures of this type to perform complex signal processing functions at the speed of light. Vibration is also not a problem due to the integrated nature of these low cost devices.

Examples in which a significant amount of improvement can be expected through guided-wave optical processing include complex signal processing tasks such as analog-to-digital conversion. Analog-to-digital converters are necessary interfaces to convert analog quantities (continuous both in time and amplitude) to their corresponding sampled digital quantities (represented by a finite number string) and are critical building blocks for radar, communications, and electronic warfare applications. All-electronic high resolution converters require a large number of comparators and have problems with crosstalk between the analog voltage to be converted and the digital output signals. Most importantly, their speed is not high enough to handle high frequency signals such as radio waves and microwaves. This latter problem places a major constraint on the wider applications of digital technology.

The electro-optical guided-wave techniques for analog-to-digital conversion can solve the problems associated with the all-electronic converters and provide an attractive alternative. These methods are based on parallel configurations of optical guided-wave interferometers. In 1978, H. F. Taylor recognized that the periodicity of the output of B interferometers (with proper length) was analogous to the periodic variation of a B -bit binary gray-coded representation of an analog quantity and that the interferometer could therefore be the basis for an analog-to-digital converter [2].

Separation of the sampling signal from the analog voltage to be digitized, elimination of the sample-and-hold circuitry, and the high speed offered through optics makes this an attractive alternative.

One of the major limitations associated with this type of approach, however, is the achievable resolution. For the folding periods to be a successive factor of 2, the length of each electrode must also be doubled. That is, an 8-bit ADC using the previous scheme would require 8 interferometers with electrode lengths of $L, 2L, 4L, \dots, 128L$ with the length of each interferometer $128L$. This electrode length doubling requirement adversely affects the device capacitance and ultimately constrains the achievable resolution [3–6].

1.3 Principal Contributions of this Research

The principal contributions of this research (October 1993–September 1994) lie in the design and development of guided-wave optical architectures for high resolution analog-to-digital conversion and the optical telemetry of the corresponding bits below deck. As the levels of monolithic integration in this technology continue to rise, it is anticipated that these types of architectures will take advantage of the the speed and parallelism offered through optics to provide a more efficient means of processing the antenna signals. This research provides the design for an optical digital link capable of 14 channel transmission. Also provided is the design and construction of two high resolution, wideband optical ADC's; (1) an 8-bit ADC with a sampling frequency of 5 MHz (prototype) and (2) a 14-bit ADC with a sampling frequency of 5 MHz. The ADC architectures incorporate high-resolution symmetrical-number-system (SNS) encoding into an analog preprocessing scheme which substantially reduces the number of comparators required for any desired resolution (resolution greater than one bit

per interferometer). It is anticipated that these hybrid SNS ADC architectures will not only enable a wideband processing capability, but, by combining the best of both worlds, also will be able to provide a high degree of precision. That is, with the combination of high speed (but low precision) optical processing and low speed (but high precision) digital processing, these architectures can provide a higher performance than either technology acting independently. In summary, the advantages of the optical SNS ADC approach over all other methods are: (1) isolation of the sampling mechanism from the analog signal; (2) a digitization of wide bandwidth signals; (3) an efficient sampling process (i.e., a sample-and-hold circuit is not required); (4) minimum number of comparators required, and (5) a corresponding high resolution capability.

1.4 Report Outline

The material presented in this report is sectioned into six parts. Section 2 provides details on the SNS preprocessing and discusses some of the important issues involved with our SNS ADC development. In Section 3, the 8-bit SNS ADC with sampling frequency $f_s = 5$ MHz is discussed. We review the status of the hardware construction and show the results from a preliminary test and evaluation. In Section 4, the 14-bit SNS ADC with $f_s = 5$ MHz is discussed and the status of this development is reviewed. Section 5 presents the digital optical link to carry the bit patterns below deck. Section 6 concludes with a discussion of the advantages of our approach and presents a schedule for the upcoming demonstrations and future efforts.

2 SYMMETRICAL NUMBER SYSTEM ADCs

SNS preprocessing techniques decompose the analog amplitude analyzer operation into a number of sub-operations (moduli) which are of smaller computational complexity. Each sub-operation symmetrically folds the amplitude of the analog signal with folding period equal to twice the moduli. Thus, each sub-operation only requires a precision in accordance with that modulus, not the amplitude of the signal. A much higher resolution is achieved after the N different SNS moduli are used and the results of these low-precision sub-operations are recombined. By incorporating the SNS folding concept, the dynamic range of a specific configuration of folding periods and comparator arrangements can be analyzed exactly.

A block diagram of the SNS ADC architecture is shown in Figure 2. The analog signal to be digitized is applied in parallel to N folding circuits (interferometers). Each folding circuit symmetrically folds the amplitude of the analog signal with folding period $2m_i$ where m_i is one of N pairwise relatively prime moduli. The symmetrically folded output from each channel is then mid-level quantized using $m_i - 1$ comparators. The SNS encoded input signal from each channel is recombined (e.g., in a programmable logic array) to derive a more convenient decimal output. The (normalized) dynamic range that can be represented unambiguously with the N moduli channels is $M = \prod_{i=1}^N m_i$. Further details on the SNS preprocessing can be found in [7–13].

2.1 Sampling Issues

For traveling wave (velocity matched) modulators, the required drive voltage to symmetrically fold the analog signal is small. Also, the input signal frequency is not a limitation since these thermally stable modulators can be driven up to 40 GHz with

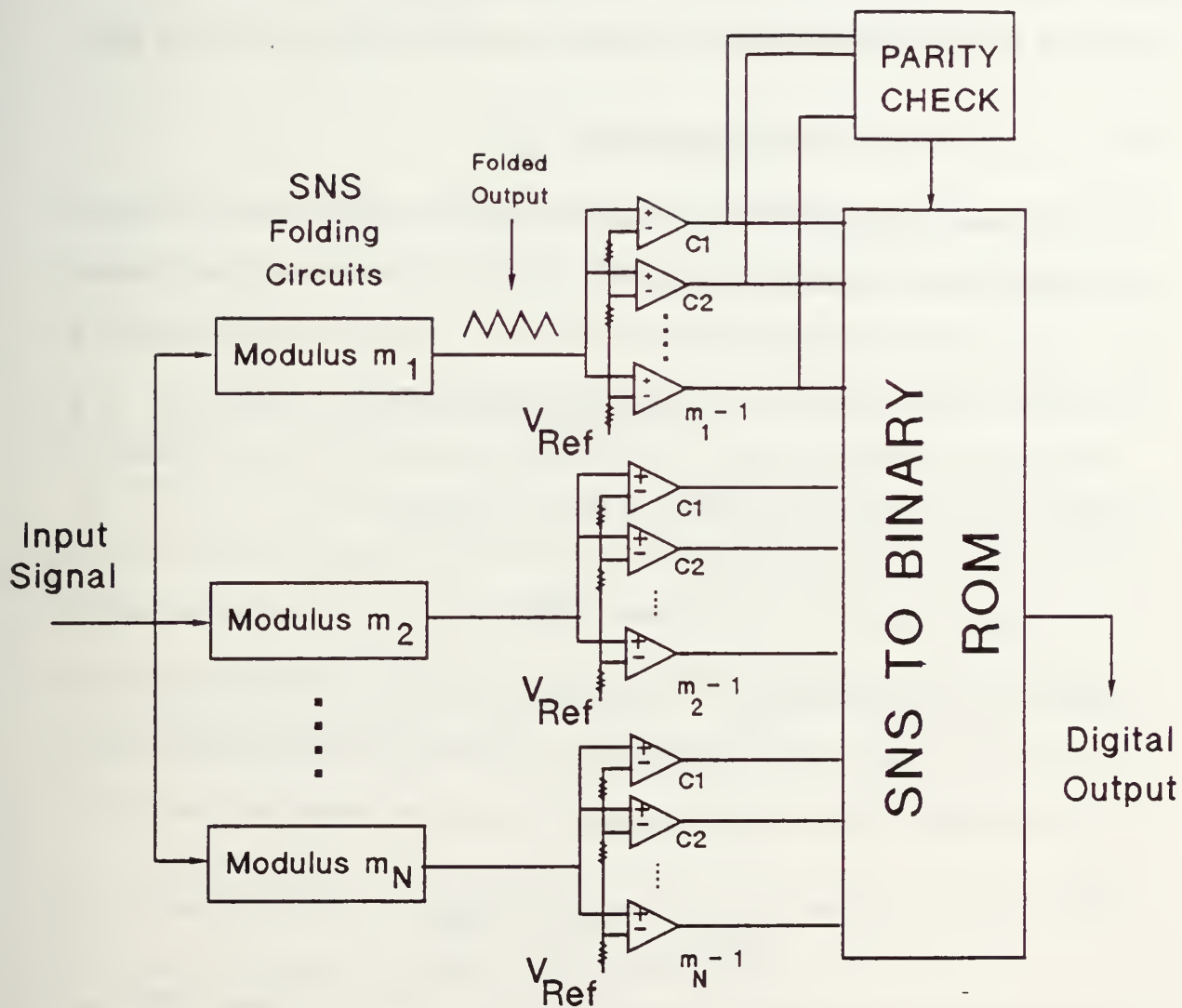


Figure 2: Block diagram of the SNS ADC architecture.

minimum attenuation [14]. The maximum frequency of the input signal does, however, affect the sampling requirements (as does the bit rate being achieved). Other than the Nyquist criteria, parameters such as the laser pulse width and the allowable sample time fluctuation (jitter) are of interest and are determined only by the sampling process. These issues, as they relate to the SNS ADC, are discussed next.

2.1.1 Laser Pulse Width Requirements

Each sample in the SNS ADC is an average of the input voltage over the finite width of the laser pulse. Through an analysis of the error in the sampled input voltage due to the total electro-optical interaction time ΔT , a maximum pulse width for a specified maximum modulation frequency can be determined.

The extent to which an error in the voltage conversion $\delta\nu$ can be tolerated is usually taken to be less than one-half of the level spacing or

$$|\delta\nu|_{\max} < \frac{V_{\max}}{2^B}, \quad (1)$$

where B is the number of bits. The maximum error due to the finite duration of the total electro-optical interaction depends on the maximum modulating frequency f_{\max} , the duration of the interaction ΔT , and the maximum voltage level and is given as [2]

$$|\delta\nu|_{\max} = \frac{(\pi f_{\max} \Delta T)^2 V_{\max}}{6}. \quad (2)$$

Substituting the level spacing criteria, the interaction time (or pulse width) must satisfy

$$\Delta T < \frac{\left(\frac{3}{2^{B-1}}\right)^{1/2}}{\pi f_{\max}}. \quad (3)$$

For example, to digitize a maximum frequency of 5 MHz with 10-bit resolution, the

maximum pulse width allowed is ≈ 5 ns. Figure 3 shows this relationship as a function of the number of bits $B \in \{8, 14, 16\}$.

2.1.2 Sample Time Fluctuation

Using Eq. (1), the maximum fluctuation in the sampling interval (jitter) is

$$\delta t_{\max} < \frac{1}{2^{B+1}\pi f_{\max}}. \quad (4)$$

For a 10-bit system with a maximum frequency of 5 MHz the maximum fluctuation in the sampling interval is $\delta t \approx 31$ ps. This relationship is shown in Figure 4 for $B \in \{8, 14, 16\}$.

2.2 Interferometer Considerations

The SNS ADC employs integrated optical interferometers to preprocess the analog signal. Each interferometer folds the input signal amplitude at a particular pairwise relative prime modulus m_i and a small comparator ladder is used after each detector to detect the various voltage levels and encode the input signal into the SNS format. The normalized interferometer output can be expressed as

$$I = \frac{1}{2} + \frac{1}{2} \cos[\Delta\phi(\nu) + \pi]. \quad (5)$$

The voltage-dependent phase shift $\Delta\phi(\nu)$ for a push-pull electrode configuration can be expressed in terms of the electro-optic parameters as [11]

$$\Delta\phi(\nu) = \frac{2\pi n_e^3 r \Gamma L_i \nu}{G \lambda}, \quad (6)$$

where n_e is the effective index of the optical guide, r is the pertinent electro-optic coefficient, G is the interelectrode gap, Γ is the electrical-optical overlap parameter, and λ is the free-space optical wavelength. These values are shown in Table 1 for

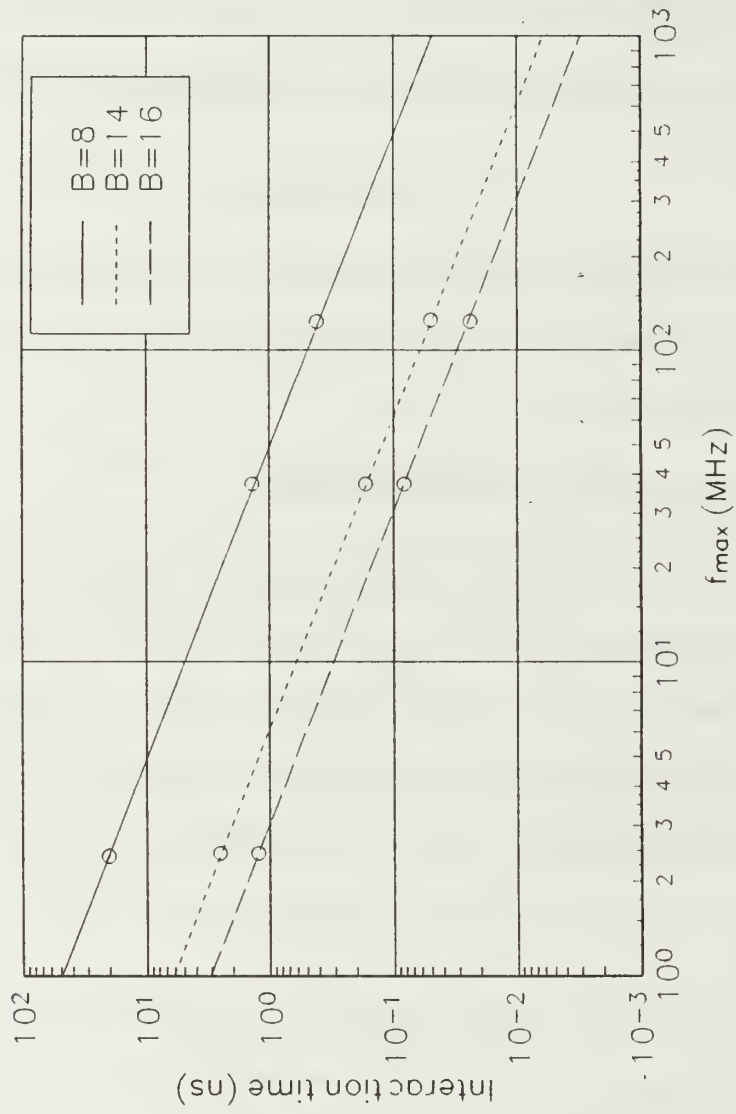


Figure 3: Interaction time for $B \in \{8, 14, 16\}$ bits.

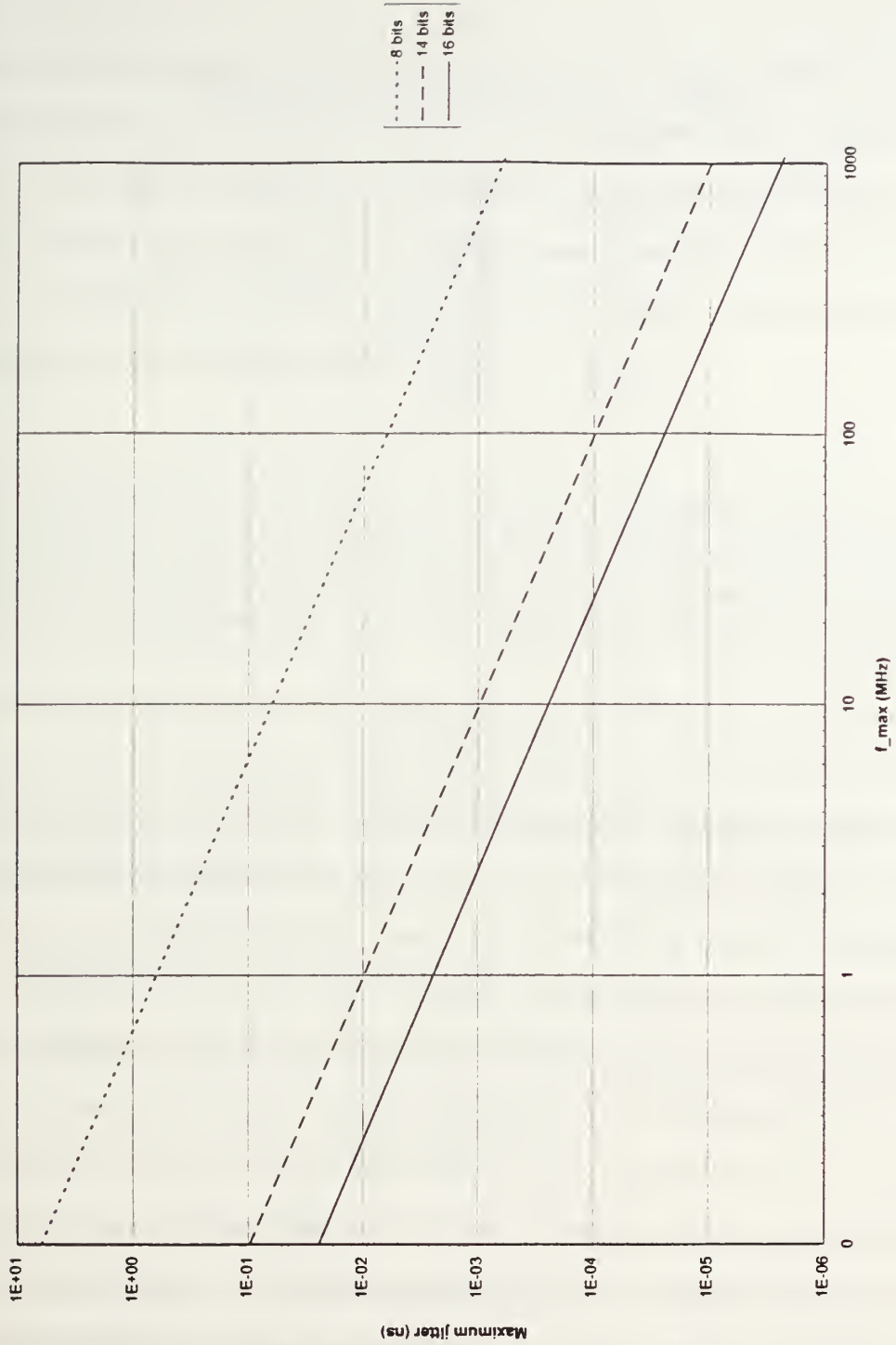


Figure 4: Maximum fluctuation in the sampling interval.

Table 1: LiNbO₃ Interferometer Parameters

G	3.0 μm
λ	0.9 μm
n_e	2.205
r	30.8×10^{-12} v/m
Γ	0.5
L	14×10^{-3} m
V_{max}	± 35 v

a typical LiNbO₃ realization. One important performance specification for an integrated optical interferometer is the amount of electrode voltage needed to transition the normalized output from a minimum ($\Delta\phi = 0$) to a maximum ($\Delta\phi = \pi$). The voltage V_π is

$$V_\pi = \frac{G\lambda}{2L_i n_e^3 r \Gamma}. \quad (7)$$

Another device constraint is the maximum voltage that may be applied to the electrodes. An applied voltage beyond the rated maximum (minimum) will spark across the electrode structure and damage the device. The specifications of V_π and V_{max} reveal the maximum number of folds available from the device. A complete fold is $2V_\pi$. The maximum number of folds F available from a device is, therefore,

$$F = \frac{2V_{\text{max}}}{2V_\pi} = \frac{V_{\text{max}}}{V_\pi}. \quad (8)$$

For the device parameters given in Table 1, $V_\pi = 0.58$ V and $F = 60$.

The smallest modulus within the SNS system requires the largest number of folds to instrument the desired dynamic range M . Since a complete fold is $2V_\pi = 2m_i$, the largest number of folds required from an interferometer in a B -bit SNS ADC is

$$F_{\text{req}} = \frac{2^B - 1}{2m_{\text{min}}} < \frac{V_{\text{max}}}{V_\pi}, \quad (9)$$

where m_{\min} is the smallest modulus in the SNS system. Consider, for example, a 10-bit system with $m_1 = 9$, $m_2 = 10$, and $m_3 = 13$. If the interferometer is that given in Table 1, the modulus 9 interferometer (m_{\min}) must fold at least $1023/2(9) \approx 57$ times, which is within the limitations of the interferometer. The modulus 10 interferometer requires 52 folds and the modulus 13 interferometer requires 40 folds. The size of the least significant bit (LSB) in an SNS ADC is

$$LSB_{SNS} = \frac{V_{\pi i}}{m_i} \quad (10)$$

where $V_{\pi i}$ and m_i are the corresponding voltage and modulus for any one of the N channels. There is a good amount of flexibility between the number of comparators required and the corresponding required number of folds. That is, for a particular resolution, an increase in the required number of folds results in a decrease in the minimum modulus and, consequently, a decrease in the required number of comparators. Depending on the hardware constraints, this type of flexibility can be used to further optimize the SNS ADC design.

2.3 Encoding Error Correction

Within the SNS ADC, the folding waveforms and comparator levels together divide the input voltage into M regions of equal size, known as the least significant bit (LSB). The points at which the folding waveforms in each channel cross the comparator thresholds all occur at the same input voltage (LSB transition voltage). The SNS can present a problem at each of these specific LBS transition voltage levels. The threshold levels need to be crossed simultaneously for several or all moduli. When some comparators, at a position to change, do change, while others do not, the recovered amplitude vector will have a large error. The probability of this occurrence depends on the offset voltage match of the comparators, the tolerance of the voltage

dividing resistors, and the corresponding width of the input voltage region being affected. In other words, we can accept the fact that a small portion of the sampled voltage levels will fall in this critical range and give false amplitudes.

The other alternative is to discard the errors using a few additional comparators. On the least modulus m_{\min} , we use $2m_{\min}$ comparators rather than $m_{\min} - 1$ (see Figure 2). Of these, $2m_{\min} - 2$ would be paired, one just below the proper comparator threshold level and the other just above. Of the other two, one would be just above the minimum modulation depth and the other threshold just below the maximum detector output. Let us assume that signal arrives and all comparators below a certain level are on. This is as it should be. For each incoming signal, if it turns on an even number of comparators, $0, 2, 4, \dots, 2m_{\min}$, the signal is rejected (decimated). If it turns on an odd number of comparators, it is accepted. In this manner we place a narrow band around each voltage level that corresponds to a switching point. For all other moduli, the comparator levels are adjusted so that they fall within these narrow bands. This is shown in Figure 5 for $m_1 = 4$, $m_2 = 5$, and $m_3 = 7$. Any input signal within these narrow rejection bands can be easily discarded.

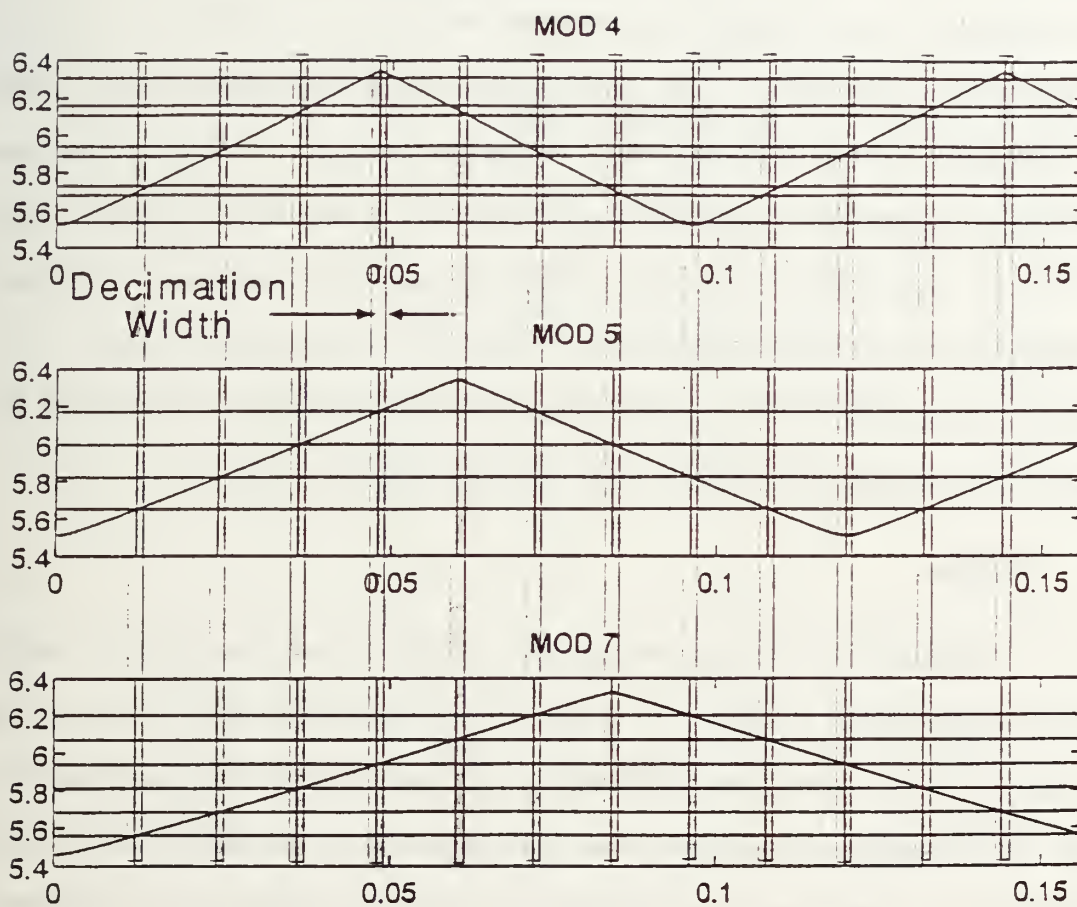


Figure 5: $2m_{\min}$ additional comparators to decimate encoding errors.

3 8-BIT SNS ADC

3.1 Design Considerations

The 8-bit SNS ADC constructed has a sampling frequency $f_s = 5$ MHz and contains three parallel channels. The three interferometers being used were built by the Naval Research Laboratory and are on loan from the National Security Agency. The maximum voltage that can be applied to these devices is $V_{\max} = \pm 30$ volts. The V_π is 2.1 volts (minimum modulus). The total number of folds available from each device is 14. Using (9), the minimum modulus is calculated as $m_{\min} = 9$. Since the channel moduli must be pairwise relatively prime the remaining two channels are $m_2 = 10$ and $m_3 = 11$. From (10), the size of the LSB is 233 mv. Including the few additional comparators for error decimation, the total number of comparators required is 37, with a maximum of 18 loaded in parallel. From (3) the pulse width required is 20 ns. From (4) the maximum fluctuation in the sampling interval is 0.25 ns.

3.2 Status

The 8-bit 5 MHz SNS ADC is near completion. All digital boards are built and tested and are currently being integrated to the optical processor front end. For the optical processor, we have ordered two additional optical receivers and three wideband amplifiers. A preliminary low-frequency test was performed on the digital boards using LabViewTM to emulate the three interferometer output waveforms. Three different transfer functions corresponding to each simulated modulation output, are shown in Figures 6, 7, and 8. In these three cases the decimation width was 0% of the LSB (no decimation). Note the presence of the encoding errors. In Figure 9, the decimation width is increased from 0% of the LSB to 10% of the LSB. Note the decrease in the number of errors present. The 14 missed code steps that appear at regular intervals

are due to an incorrect matching voltage on the lower decimation comparators which has since been corrected. Figure 10 shows the transfer function for a decimation width of 15% of the LSB. The number of errors present is further decreased. The transfer function for a decimation width of 20% of the LSB is shown in Figure 11. Note the absence of any encoding errors.

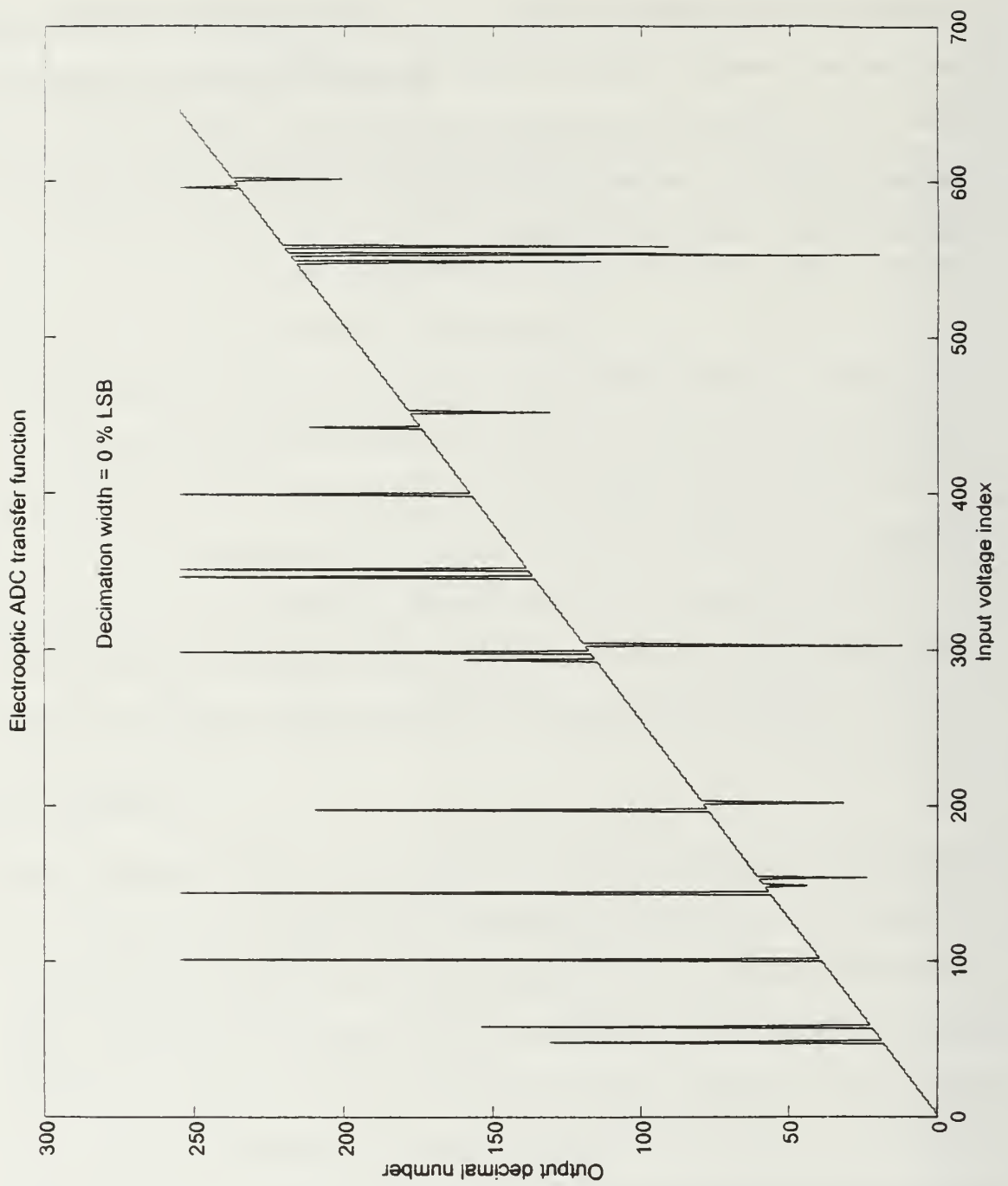


Figure 6: Transfer function with 0% LSB decimation width.

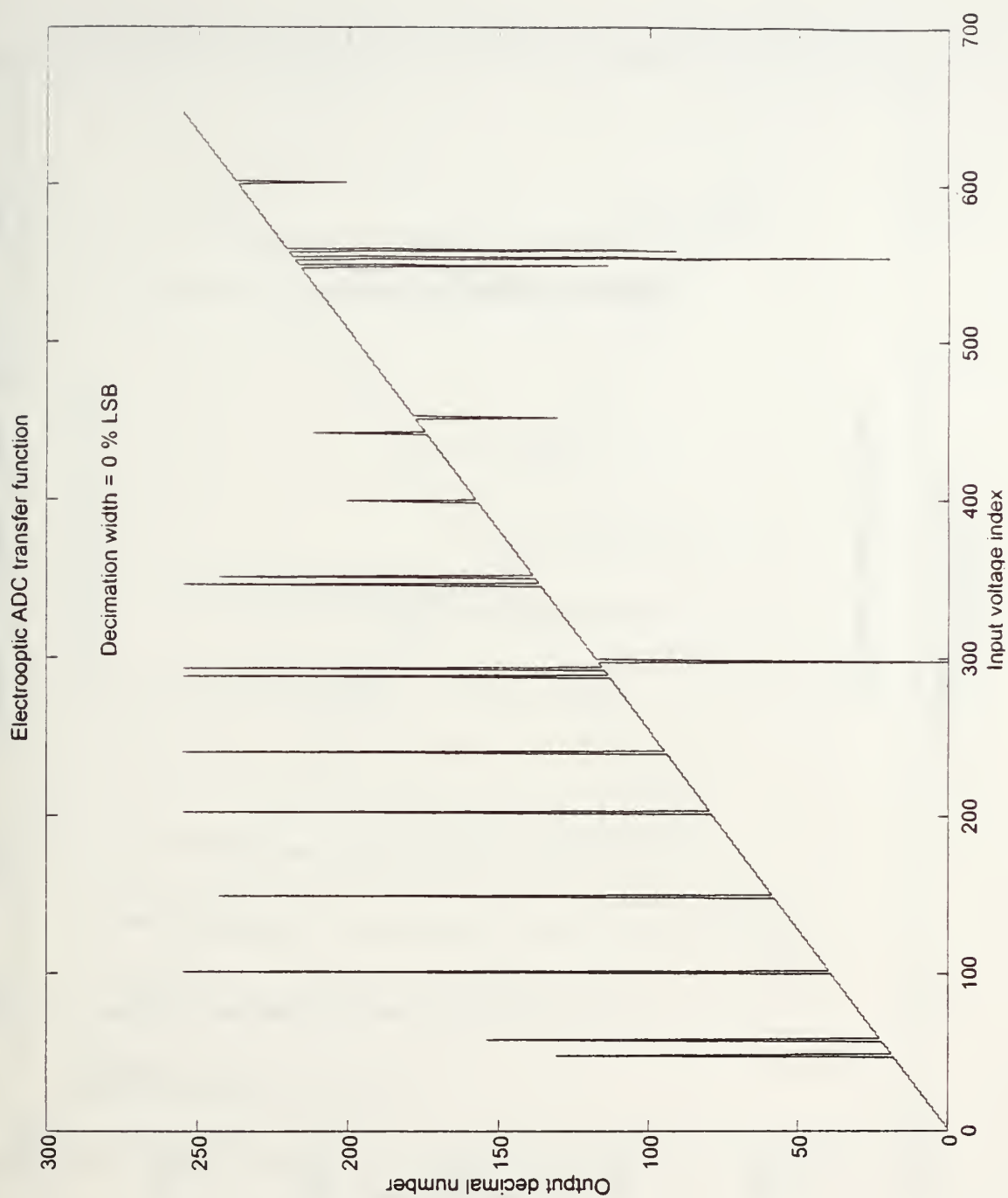


Figure 7: Transfer function with 0% LSB decimation width.

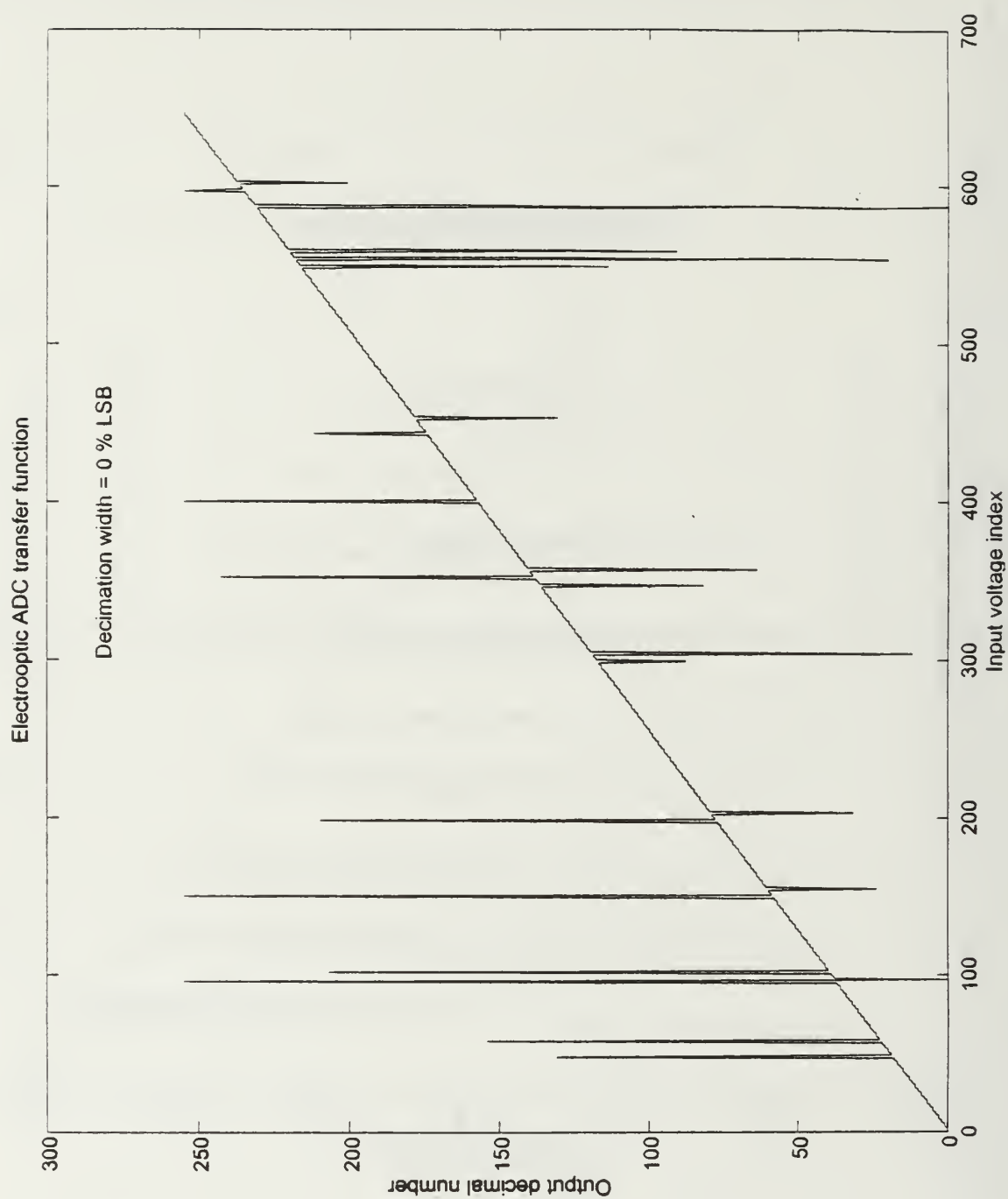


Figure 8: Transfer function with 0% LSB decimation width.

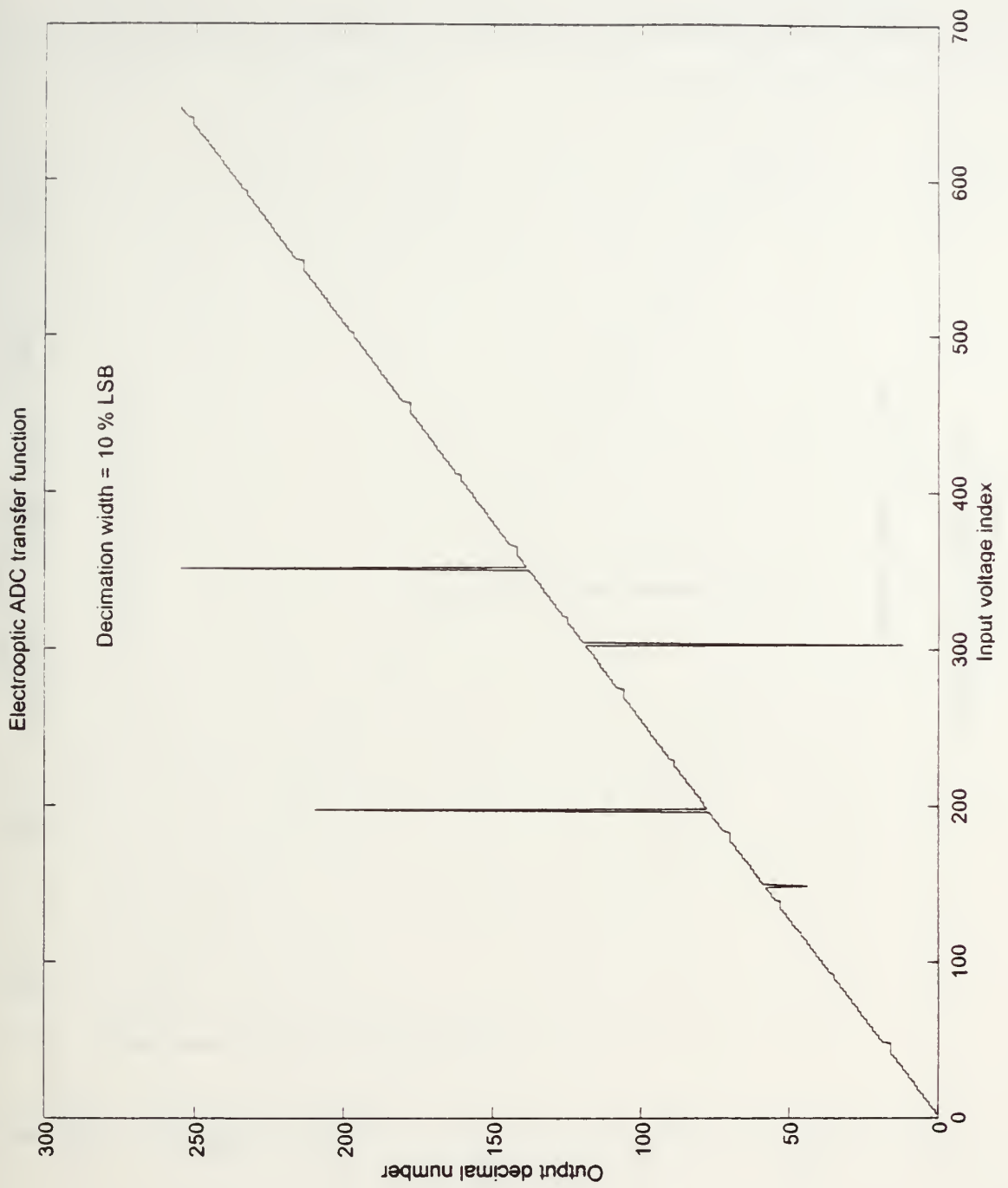


Figure 9: Transfer function with 10% LSB decimation width.

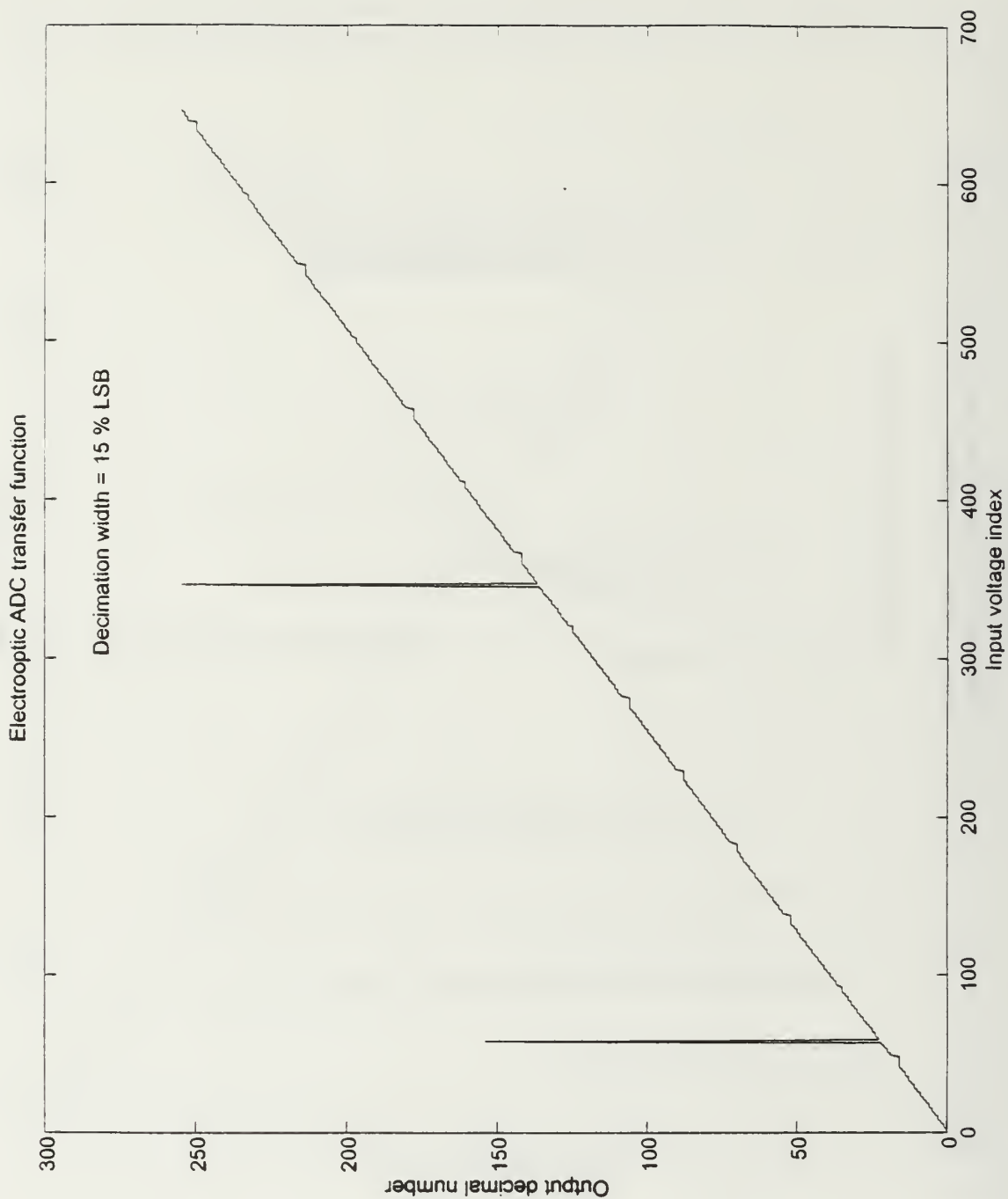


Figure 10: Transfer function with 15% LSB decimation width.

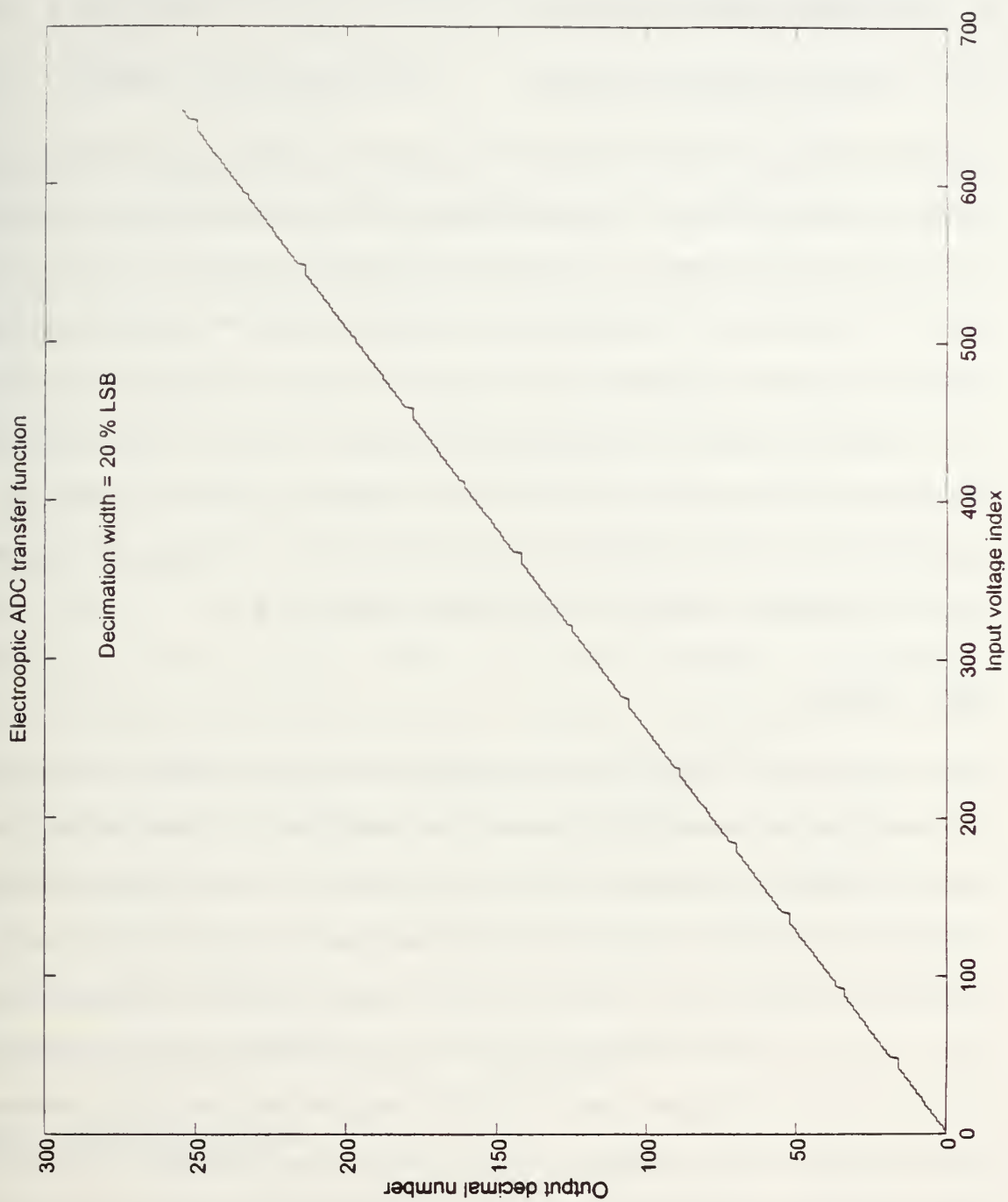


Figure 11: Transfer function with 20% LSB decimation width.

4 14-BIT SNS ADC

4.1 Design Characteristics

The 14-bit design with $f_s = 5$ MHz is a straight forward extension of the 8-bit architecture discussed above. The interferometers being used for this device are built by United Technologies Photonics and have a maximum voltage of $V_{\max} = \pm 50$ volts and a V_π of 0.35 volts. This results in 142 folds available. With 142 folds, the minimum modulus is calculated to be $m_{\min} = 59$. Since the channel moduli are pairwise relatively prime, the system configuration is $m_1 = 59$, $m_2 = 60$, and $m_3 = 61$. The size of the LSB is 6 mv. The total number of comparators required is 237 with a maximum of 118 loaded in parallel. The pulse width required is calculated to be 2.5 ns and the maximum fluctuation in the sampling interval is 4 ps.

4.2 Status

In this configuration, to eliminate any transient time mismatch between the detected laser pulse and the comparators, printed circuit boards are being designed with an expected completion date of April 1995. For the optical processor, we have purchased three reflective interferometers from United Technologies Photonics, they are expected to arrive by the end of January 1995. To couple the signal into and out of the reflective design, three optical circulators are also on order from E-Tek Dynamics. These devices should arrive during the first quarter of 1995. Integration with the digital processor should take place in June 1995 with a full up demonstration scheduled for July 1995.

5 14-CHANNEL OPTICAL DIGITAL LINK

5.1 Design Considerations

The feasibility of transmitting the 8 or 14 bits at a high speed over a fiber network in the subject of this section [15]. The parallel outputs of the SNS ADC are connected to an optical transmitter, which serializes the data and transmits the serial data to an optical receiver below the deck through a high-speed fiber link. The optical receiver converts the data back to a 14-channel parallel data word and sends it to the signal processing units. This optical digital link configuration is shown in Figure 12.

To date, the optical transmission of the data over a high speed optical link has not yet been examined. The parallel data from the SNS ADC are converted to a serial data by the use of a special parallel-to-serial converter. The serial data are transmitted through a wire link with a design bit rate of 70 Mbps. A block diagram of the transmitter-receiver system is shown in Figure 13. At the other end of the link, the receiver receives and converts the serial data back to parallel form with a serial-to-parallel converter. The ultimate data transmission will occur over an optical link, as shown in Figure 14. The serial data from the transmitter modulates the optical source, which is then introduced to a fiber link. At the receiver end of the link, an optical detector receives the retrieves the serial data. The serial data is ultimately converted back to parallel form with a serial-to-parallel converter.

5.2 Requirements

In addition to the data transmission line, two other links between the transmitter and the receiver need to be used to guarantee the correct data reception. These links are the clock signal and a sync pulse. However, there are techniques to embed the clock and the sync pulse into the same link with data, but the overhead of this is to at

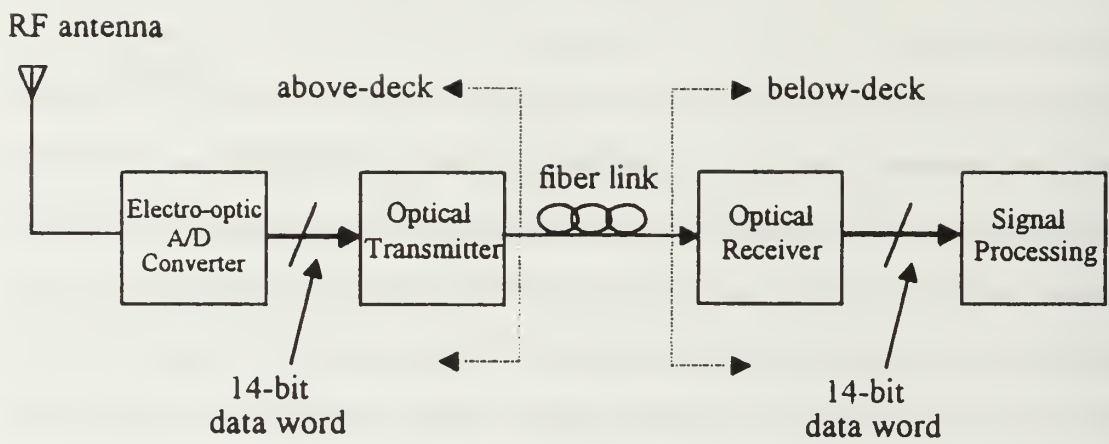


Figure 12: Optical digital link.

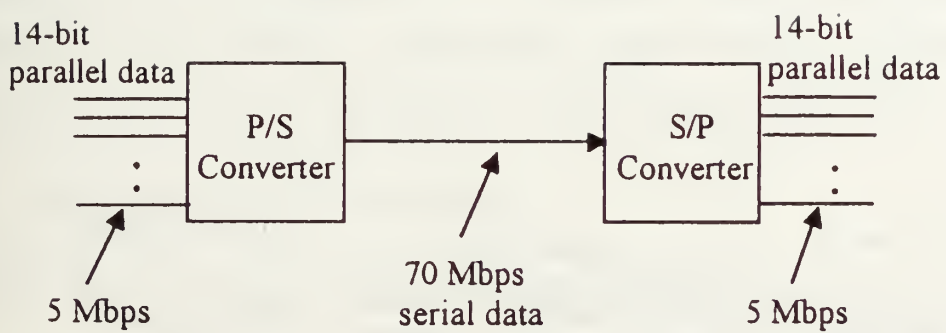


Figure 13: Block diagram of the transmitter-receiver system.

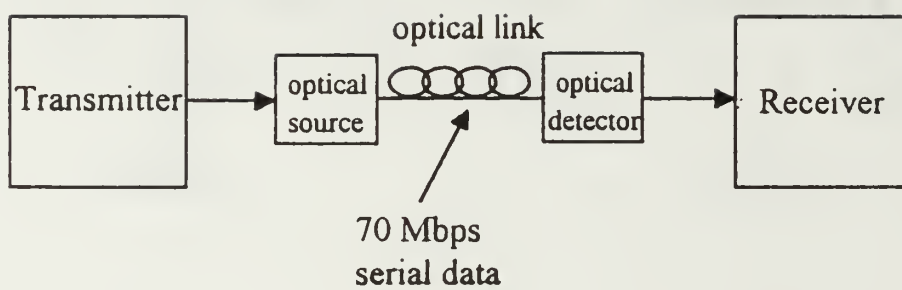


Figure 14: Optical transmission of the data.

least double the bit rate in the serial data channel. Figure 15 shows this architecture in detail. The high speed data rate which is used forces the use of “emitter-coupled logic” in the circuit design. ECL is today’s fastest form of silicon-based digital logic. The high speed rise times, low propagation delays, and very short setup/hold time of the ECL devices make them very suitable for high-speed, high-frequency logic design. The saturated logic families, such as TTL, do not meet the requirements for a high frequency logic design.

A crystal oscillator is used to generate a 70 MHz clock which provides a signal that is free from noise. The integrated circuit oscillators of the ECL family have very fast edge speeds which cause distortion due to reflections on signal lines. This feature requires utilization of some special interconnection and wiring techniques, which limit the flexibility of the implementation. Our application does not require such fast edge speeds, so a crystal oscillator, which provides a signal which has a somewhat slower edge speed but is free from distortion, is a better choice for this research.

5.3 Multiplexing Techniques

Multiplexing is a technique to share a single data link among multiple data channels. As depicted in Figure 16, n inputs are accepted by the multiplexer and combined into a single high-capacity data link. The demultiplexer at the other side receives the data stream. Multiplexing techniques can include:

- frequency-division multiplexing (FDM),
- code-division multiple-access multiplexing (CDMA),
- wavelength-division multiplexing (WDM), and
- time-division multiplexing (TDM).

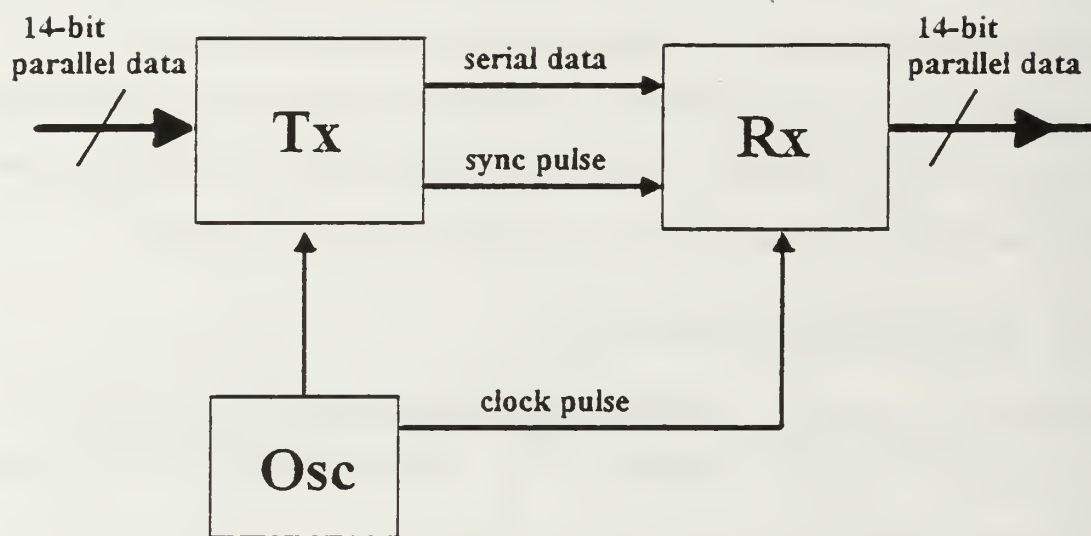


Figure 15: Links between transmitter and receiver.

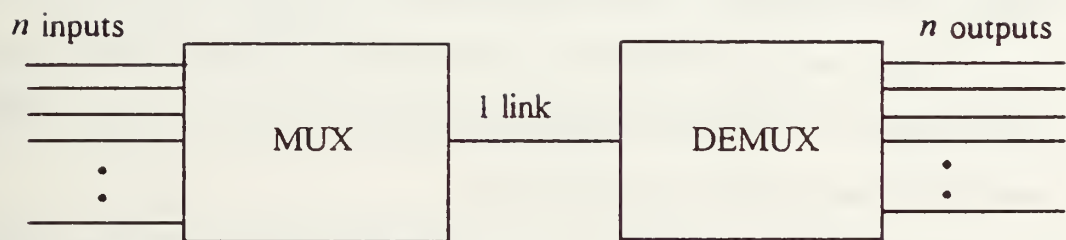


Figure 16: Multiplexing and demultiplexing.

We have chosen TDM. TDM assigns different time intervals to the individual signals and transfers them to the transmission link one-by-one in physically different time intervals. The same frequency and the same coding/modulation technique can be used for all signals.

5.4 Status

This research accomplished the goal to serialize 14-channel digital data with a bit rate of 5 Mbps and to transmit them at 70 Mbps. The transmitter has a flexibility of changing the bit rate easily. The receiver, however, was not able to catch the data in correct sequence with 70 Mbps. The setup and hold time of the buffer in the receiver was not short enough for an incoming data with a period of 14.3 ns. The receiver received the data correctly below 39 Mbps and converted them back to parallel form. Above that bit rate, there was a flickering and unstable data at the output.

Some faster devices with a shorter setup and hold time are being investigated to accomplish 70 Mbps reception. For example, the MC10H176 from the MECL10KH family can be used instead of MC10176. The MC10H176 has a setup time of 1.5 ns and a hold time of 0.9 ns, whereas MC10176 has a 2.5 ns and 1.5 ns setup and hold time, respectively, according to the specifications.

The clock pulse and the sync pulse can be embedded into the same transmission line with the serial data using some special techniques to avoid the need for extra links between the transmitter and the receiver. However, this will double the bit rate to 140 Mbps. An alternative design utilizing a commercial high-speed VLSI communications chip is also being considered.

6 SUMMARY

The advantages of the integrated optical SNS approach to ADC design over the all-electronic approach include: (1) isolation of the sampling mechanism from the analog signal; (2) a digitization of wide bandwidth signals; (3) an efficient sampling process (i.e., a sample-and-hold circuit is not required); (4) minimum number of comparators required, and (5) a corresponding high resolution capability.

The 5 MHz 8-bit device will be demonstrated in the first part of 1995 and the 5 MHz 14-bit device will be demonstrated towards the middle of 1995. The optical digital link will also be demonstrated. Along with the demonstration, we will also be performing a series of tests specified by MIT Lincoln Laboratory to evaluate the device performance. Planned tests include

- 1) Frequency domain
 - a) Single-tone DFT
 - b) Two-tone DFT
- 2) Single-tone spurious-free dynamic range
- 3) Histogram
- 4) Residual error
- 5) Two-tone intermodulation-free dynamic range
- 6) Noise power ratio

It is expected that the test results and demonstration will detail the advantages of our approach and demonstrate a clear advantage over current methods of shipboard antenna signal processing.

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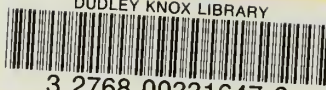
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