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ILLIAC III: A PROCESSOR OF

VISUAL INFORMATION

by

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June 10, 1965

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cop.3 An outline for visual data processing using the Illinois Pattern Recognition Computer (ILLIAC III) is presented. The input image is digitized by a TV-like scan, then digitally filtered and idealized to a line drawing in the Pattern Articulation Unit. Upon output from this unit the image is described by a string of displacement vectors, appropriate for an incremental plotter with coordinate stack storage. Subsequent recognition consists of programmed syntactic and semantic analysis of the vector string description¹ using an enriched repertoire of list processing instructions.

1. Computer Organization

ILLIAC III is a multi-processor computer system. Eight terminal groups [Taxicrinic Units (4), Monitor Control Units (2) and I/O Channel Control Units (2)] access in parallel the centralized processors of the computer (Figure 1).

These centralized processors include the three storage groups. Each storage group consists of a fast core module (16,384 double words, 1.2 μ sec), a slow core module (65,536 double words, 4 μ sec), and a dictionary (fast mostly-read memory). A final group of shared processors includes two arithmetic units² and the novel parallel processor for visual data processing--the Pattern Articulation Unit.

Visual input to the computer enters through flying spot CRT scanners: two for 70-mm film, two for 46-mm film, two for 35-mm film and two for microscope slides. Two modes of raster scanning are provided: <u>raster</u> <u>mode</u>, where cell-by-cell the image is encoded uniformly in 1, 2, 4, or 8 bits of gray scale; and <u>coordinate mode</u>, where each black/white transition triggers the readout of 16-bit X(Y) coordinates. Raster mode is the normal recognition scan input; coordinate mode is primarily reserved for precision measurement purposes.

^{1.} Narasimhan, R. "Labeling Schemata and Syntactic Descriptions of Pictures," <u>Information and Control</u>, Vol. 7, pp. 151-179, (1964).

^{2.} Robertson, J. E. "Methods of Selection of Quotient Digits During Digital Division," IFIP Paper. May 23-29. 1965, New York.

Visual output of the computer again uses the film scanners, which can also operate as film cameras. Display modes include the write version of the raster and coordinate scan described above. In addition a vector display mode--where the CRT scanners operate as incremental plotters with stack memory--is provided.

To assist human intervention, monitor stations (each provided with CRT display, typewriter and incremental magnetic tape unit) are made an integral part of the system.

2. Image Idealization

Strips of the input picture are scanned (in raster mode) into fast core storage. A two-dimensional segment of the image, 32×32 bits, (called a "window") is then word-serially loaded from computer storage into the Pattern Articulation Unit (PAU). Within this processor subsequent digital idealization of the window image proceeds in parallel, (i.e., in the 1024 + 132 cell modules of the iterative array). The PAU is controlled by a string of instructions transmitted by the controlling Taxicrinic Unit (or monitor).

The input image is normally idealized to a line drawing. In particular local filtering algorithms which utilize both the stochastic characteristics of the image noise and definition of the idealized picture have been developed (see Figure 2).^{3,4} Notice the extent to which burst noise in the original image has been correctly compensated.

3. Scan Conversion: The Articulation Process

With the image idealized, the second role of the Pattern Articulation Unit can be visualized as a scan conversion: from <u>raster mode input</u> (i.e., TV-like scan) to <u>vector mode display output</u>. That is, we take a particular incremental plotting language as the primitive basis for image description.

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^{3.} Yamada, S. "Local Recognition of Pictorial Images," Department of Computer Science, University of Illinois, Urbana, Illinois. Report in preparation.

^{4.} James Fornango programmed the filtering algorithm demonstrated in Figure 2, University of Illinois, Urbana, Illinois.

The displacement vectors generated are single characters $(\pm \Delta X, \pm \Delta Y)$ with $0 \le X \le 7, 0 \le Y \le 7$. When $\Delta X = \Delta Y = 0$, the sign information is used to designate control instructions.⁵ Specifically control instructions allow one to push (pop) the current (X,Y) coordinate pair into (out of) a coordinate stack. The incremental plotting language, so interpreted, provides a compact description language for the image outlines previously created.

The mechanism of this scan conversion is the pattern articulation process illustrated in Figure 3. Here the window image has been idealized and critical nodes (i.e., basic sets) isolated by parallel processing. The crucial remaining step, we observe, is to reestablish the connectivity between these critical nodes. Connectivity of the image can be indicated by (1) listing nearest neighboring nodes to a given node, or alternately by (2) generating a vector string which, if sent the incremental plotter, would draw straight line vectors to these neighboring nodes. Both options [(1) and (2)] are provided directly by wired-in control logic of the PAU.

Figure 4 suggests schematically the critical PAU facilities that permit rapid listing of neighboring nodes. First two associated windows must be identified: (1) the idealized image and (2) the set of critical nodes of the image. The PAU through a program-controlled path building facility, allows fan out from the point of initial excitation generating the image SO. Using planewise Boolean logic the complement of the M' plane is SO \cdot $\overline{56}$. A wired-in coordinate scan then automatically lists either the coordinates of these neighboring points, or alternatively their vector string representation.

4. Current Engineering Status

Two-thirds of the Pattern Articulation Unit have now been fabricated. Each cell module (of the 1024 + 132 cells) of the iterative array is a 5"-x-5" printed-circuit card. Each card houses approximately 200 microdiodes and 45 transistors. Seven scanners and five monitors are now nearing completion.

^{5.} H. P. Peterson has implemented a related 12-bit vector display code. Control Data Corporation, Digital Graphics Division, Burlington, Massachusett

^{6.} Breeding, K. J., McCormick, B. H., and Witsken, J. R., "Order Code for the Film Scanners of ILLIAC III," Department of Computer Science, University of Illinois. Report now in preparation.

Two Taxicrinic Units are under construction. These units provide list processing instructions, memory protection, and the facility to directly execute without programmed intervention all macro instructions satisfying certain formal call format conventions.

From simulation studies, processing turn of ILLIAC III for visual information can be estimated at 0.5 - 1 msec/window or approximately 1 sec for a $10^3 \times 10^3$ bit picture. We assume the material is scanned at a magnification such that window image identification is not obscured by black/white encoding of the 32 × 32 bit fragment.



SCHEMATIC OF ILLIAC III





ORIGINAL

PROCESSED

FIGURE 2. DIGITAL IMAGE FILTERING



FIGURE 3. VISUAL PATTERN ARTICULATION



FIGURE 4. ESTABLISHING LINK BETWEEN AN INITIATION NODE AND NEXT NEAREST NODES

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