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INDIRAD: A DIGITAL RECEIVER FOR AMPLITUDE MODULATED SIGNALS USING INDICATOR PROCESSING

BY

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THESIS

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1. Introduction

The purpose of this thesis is to investigate the application of Indicator processing and quadrature sampling to the reception of broadcasted signals. The results of this study were used to build INDIRAD, a true digital receiver for amplitude modulated signals.

Many "digital receivers" are actually digitally controlled analog receivers. The rejection of unwanted signals is done by voltage controlled analog filters. The controlling voltage is generated digitally from some combination of the desired station and feedback parameters. These receivers have excellent reception, but are usually very expensive.

True digital receivers first sample the analog input and then use digital filtering techniques to extract the desired station from the composite signal. One advantage of digital filtering is that filter characteristics can be realized which are unattainable with analog filters. Also, with the rapid decrease in cost of digital electronics especially in custom LSI components, a high quality digital filter may soon be less expensive than an analog one.

Many digital receivers previously built must stay phase synchronized to the carrier of the desired station in order to demodulate it. This usually requires a phase locked loop along with either a very high sampling rate or an adjustable sampling period. While this may be necessary for FM signals (even analog receivers use phase locked loops for FM), a simpler approach is described here for AM signals.

Section 2 of this paper introduces Indicator representation, processing, and encoding. Section 3 presents quadrature sampling and how it might be used to construct an AM receiver. Section 4 describes INDIRAD, the digital receiver built to demonstrate Indicator processing and quadrature sampling.

2. Indicator Processing

In conventional weighted binary numbers, log (n) bits are required to represent a variable which can have N values. As an alternative to this binary representation, a variety of unary representations have been proposed by Poppelbaum [1,2]. These require N bits to present a variable which can have N values. One of these representations, Burst Processing, has been applied to devices such as spectral analyzers [3], failsoft storage systems [4] and digital receivers [5]. Advantages of Burst Processing include simple arithmetic units and efficient encoders and decoders. However, since Burst is a unary bit serial representation, clock rates higher than those of parallel weighted binary systems are required to process the same amount of data. Indicator processing, being a unary parallel representation, overcomes this problem. This section explains Indicator representation, processing and encoding, and compares them to their weighted binary equivalents.

2.1 Indicator Representation

Indicator is a "one out of N" representation. If a variable can have N possible values, the Indicator number will have N bits or, in hardware, N wires. The bit which corresponds to the value of the variable will be "ON", while all other bits will be "OFF". Since a variable can have only one value at a time, every valid Indicator number must have exactly one bit "ON". Figur 2.1 shows a six valued variable and some valid and illegal Indicator representations. An Indicator number can be seen to be a decoded weighted binary number; i.e., the pattern which would result from a 1 to N decoder.

Value of the variable	Indicator Representation of Values			
	1	4	illegal	illegal
6	0	0	0	0
5	0	0	1	0
4	0	1	0	0
3	0	0	1	0
2	0	0	0	0
1	1	0	0	0

Figure 2.1 Indicator Representation

2.2 Indicator Arithmetic

Since Indicator is a naturally decoded representation, any arithmetic operation on two variables can be done by "table lookup". The hardware realization of this table is called an Indicator matrix. Figure 2.2 shows a three by three matrix where inputs A and B are three valued Indicator variables. The AND gate where the active bits in A and B intersect will generate an active output through the OR gate to the appropriate bit of S. This matrix generates the sum S = A + B, where S is a five bit Indicator number.

From Figure 2.2 it is obvious that the maximum time to perform an arithmetic operation will be two gate delays. If a logic family is used which allows Wire ORing, the time can be cut to a single gate delay. For 10000 series ECL this is about 2 nanoseconds. This is much faster than any weighted binary arithmetic operation could be performed.

For a Indicator matrix with inputs A and B having N values, the number of points (gates) in the matrix will be N^2. For large values of N this amount of hardware may become excessive. However if one compares the number of gate equivalences between an Indicator matrix and a binary full adder (Table 2.1), one will see that Indicator requires fewer gates for N less than or equal to 5, and less than 2.5 times as many for N between 6 and 10. Therefore for applications where high speed, low precision arithmetic is required, Indicator processing is a suitable alternative.

2.3 Generation of Indicator Values

One area where Indicator values can be naturally generated is in high speed parallel analog to digital converters. The fastest A/D converter is simply a set of comparators with monotonically increasing reference voltages, as shown in Figure 2.3. The output can always be partitioned into a set of 1's and a set of 0's. This form can easily be converted into

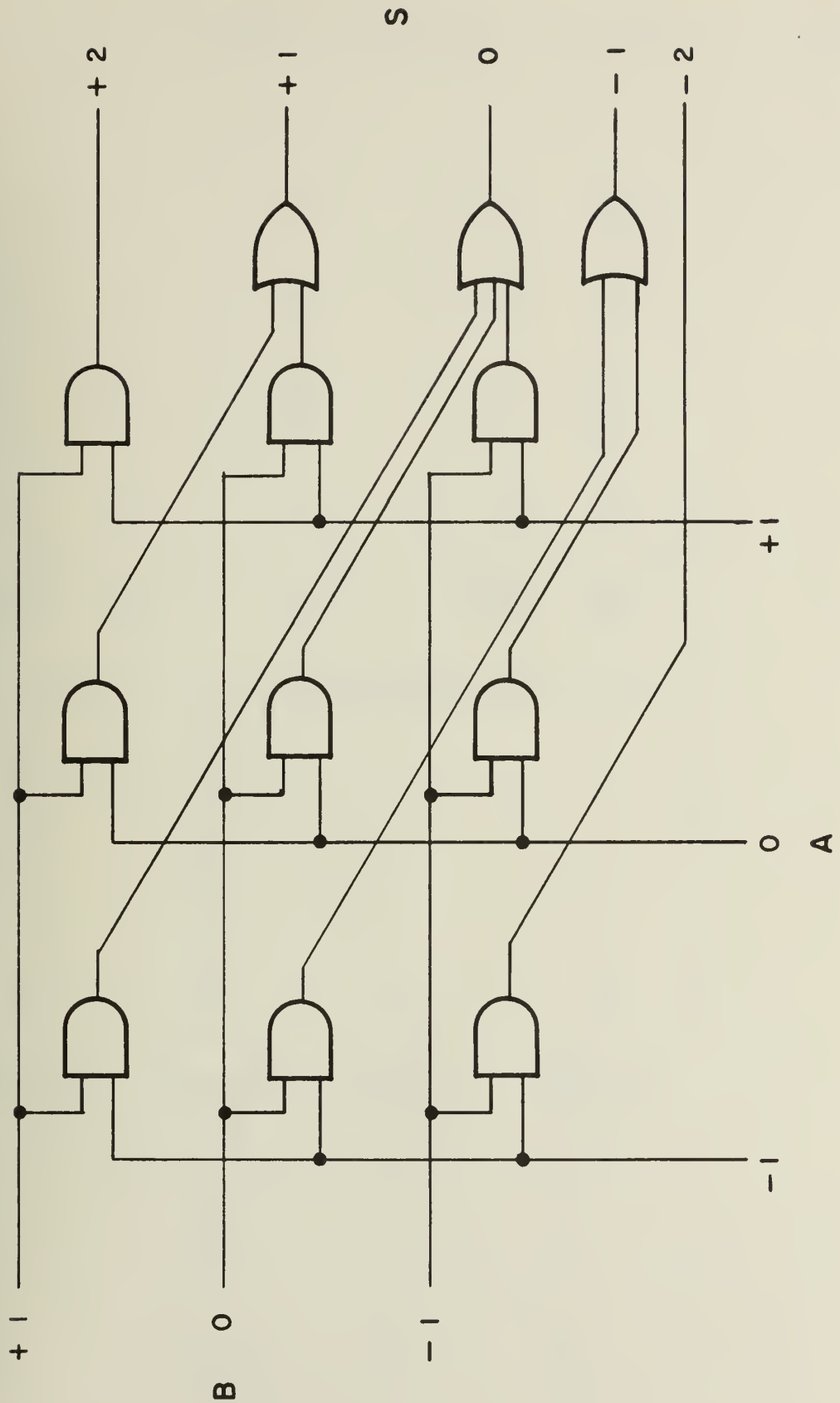


Figure 2.2 An Indicator Matrix S = A + B

Indicator Values	Binary Bits Required	Gate Equivalents Indicator	Binary
2	1	4	10
3	2	9	20
4	2	16	20
5	3	25	30
6	3	36	30
7	3	49	30
8	3	64	30
9	4	81	40
10	4	100	40
11	4	121	40

Table 2.1 Gate Equivalences

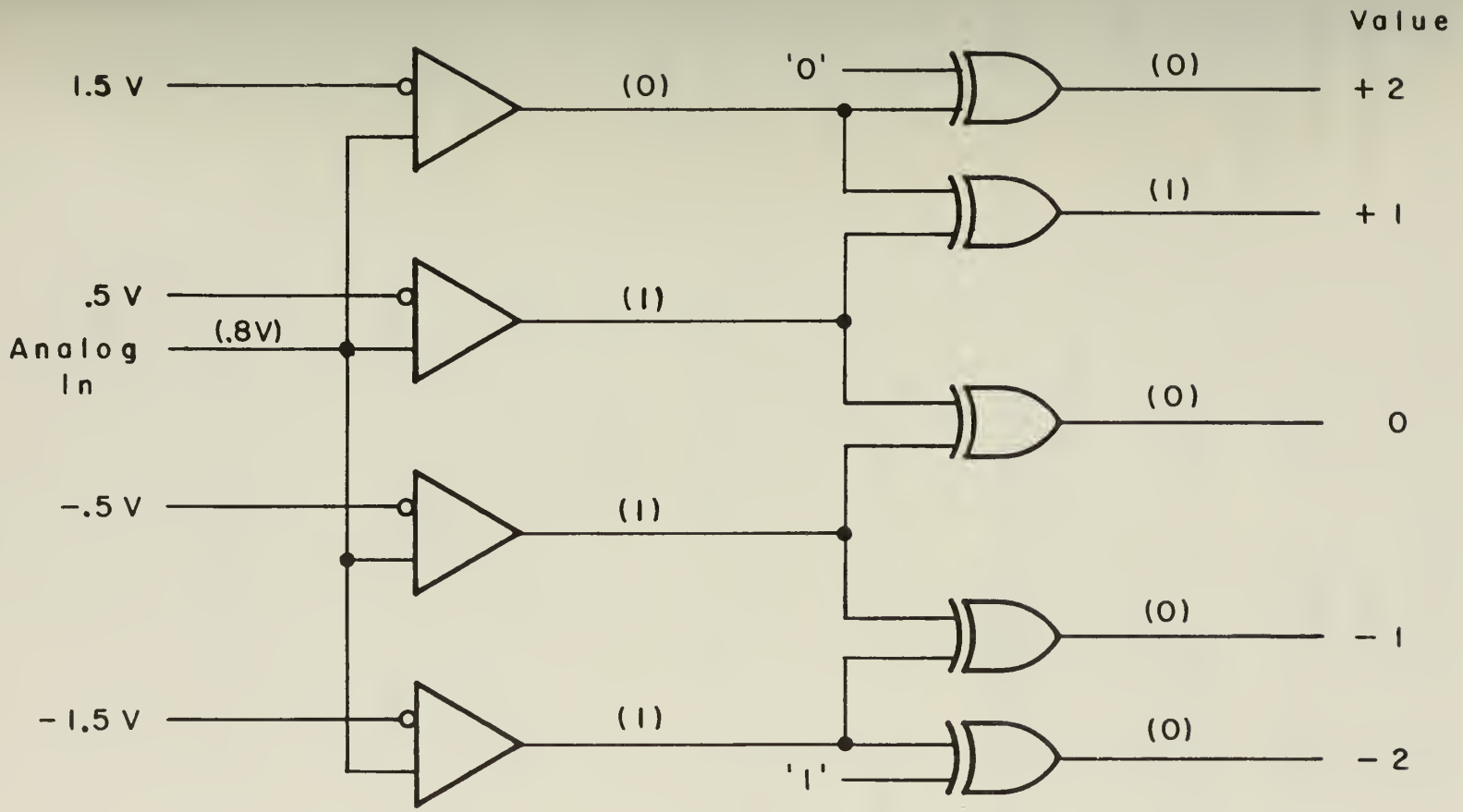


Figure 2.3 Analog to Indicator Converter

Indicator representation by pairwise exclusive ORing adjacent bits. The resulting output is in Indicator form with a 1 in the active level and 0's elsewhere.

Care must be taken in the generation of Indicator values so that illegal values do not result (Figure 2.1). One invalid input may propagate throughout the system causing erroneous results without end. This condition may also occur on power up when registers are not initialized. Depending on the system architecture, a variety of self resetting circuits can be devised which will insure that any illegal value introduced into the system will be cleared out within a certain amount of time. One example of this was incorporated in INDIRAD, and is explained in section 4.

3. Quadrature Sampling for Digital Receivers

This section will present the idea of quadrature sampling and how it may be applied to demodulation of an amplitude modulated signal. While a basic understanding of digital signal processing is assumed here, a few relevant points about aliasing and decimation will be briefly mentioned. For a thorough coverage the reader is refered to the references [6,7].

3.1 Quadrature Sampling

Assume we wish to demodulate a signle amplitude modulated (AM) signal of the form:

$$S(t) = M(t)\ SIN(2\Pi\ F_C\ t)$$

We can take advantage of the well known trigonometric formula

$$SIN^2(X) + COS^2(X) = 1$$

to find the amplitude as follows. Let us take two samples of the signal, the first sample being anywhere in time, say t_1, and the second being $1/4F_C$ seconds later. Thus these two sample are 90 degrees out of phase from each other, or are in quadrature. Assume the two samples, A and B, are of the form:

$$A = M(t_1)\ SIN(2\Pi\ F_C\ t_1 + \phi)$$

$$B = M(t_1 + 1/4F_C)\ SIN(2\Pi\ F_C\ (t_1 + 1/4F_C) + \phi)$$

If we assume that F_C is much higher than the highest frequency of M(t), then we can assume that M(t) is constant for several cycles of the carrier and can approximate it by M.

We now reduce B to:

$$B = M\ SIN(2\Pi\ F_C\ t_1 + \Pi/4 + \phi)$$

$$= M\ COS(2\Pi\ F_C\ t_1 + \phi)$$

$$= M\ COS(X)$$

Similarly, A becomes:

$$A = M \, SIN(2\Pi \, F_C \, t_1 + \phi)$$
$$= M \, SIN(X)$$

If we now square A and B and add them together we get:

$$A^2 + B^2 = M^2 \, (SIN^2(X) + COS^2(X)) = M^2$$

Now taking the square root of this we get M, the amplitude of the carrier.

Notice that the first of the samples taken can occur anywhere during a cycle of the carrier. Thus this method of peak detection is not phase locked to the incoming carrier. It has the advantage, like analog peak detection, of simplicity and speed, due to the elimination of feedback, while retaining the versatility of being digital.

3.2 Aliasing

If a bandlimited analog signal is sampled at a frequency F_S, the resulting discrete time spectrum will be a periodic repetition of the analog spectrum. The original spectrum will be repeated about every NF_S in the discrete time spectrum. If F_S is less than twice the highest frequency present in the analog signal, aliasing will occur. That is one frequency component will appear to be at a different frequency due to the overlapping of the spectra. If F_S is greater than twice the highest fequency, that is above the Nyquist rate, aliasing will not be present.

Similarly, if an infinite spectrum signal is sampled at F_S, overlapping of spectra will occur causing signals at frequencies $NF_S \pm F_C$ to be indiscriminatable from a signal at F_C. Therefore if the incoming signal is bandlimited such that only one frequency of the $NF_S \pm F_C$ frequencies is present, that frequency may be shifted to F_C by sampling it at F_S.

3.3 Decimation

Decimation is the process of decreasing the sampling rate of a discrete time signal. This would be done to a signal which has been sampled at a high rate and where the frequencies of interest are low. Decreasing the sampling rate in effect lowers the sampling frequency and thus may cause aliasing to occur. That is, high frequencies before decimation may be folded back onto the low frequencies of interest when the sampling rate is decreased.

To avoid this we must first filter the input samples so as to block any high frequencies which would fold back onto the frequencies of interest. The simplest method of doing this is to low pass filter the input. If the filter has a cutoff frequency of half the new sampling rate, aliasing will be prevented. The signal may then be decimated by simply dropping unwanted samples. For example, to decimate a signal by four, every fourth sample is passed and the rest are discarded.

In practice, there is no reason to calculate the unwanted samples in the digital lowpass. If we decimate by M, only every Mth sample need be computed. Thus we can reduce the output sampling rate, and thus the computational speed by 1/M. This is an important point to consider when choosing between an infinite impulse response (IIR) filter and a finite impulse response (FIR) filter for the digital bandpass. For an IIR filter all previous outputs are required to compute the next output. Therefore, all outputs must be calculated regardless of whether decimation is involved or not. However, any output from an FIR filter depends only on previous inputs. Since the filter itself does not need previous outputs, we are free to reduce the output sampling rate. It is therefore preferred to use FIR filters in decimators.

3.4 A Quadrature Receiver

With the foregoing as background, design of an AM receiver using quadrature sampling will now be discussed. The goal here is to devise a circuit which will accept as input samples of a bandlimited RF source. This source will be composed of many signals at different frequencies. The output will be samples of the amplitude of the desired signal. Note that the input sampling rate will be in the RF range, .5 MHz and up, while the output sampling rate will be in the audio range, and need only be about 10 KHz. Therefore decimation may be involved.

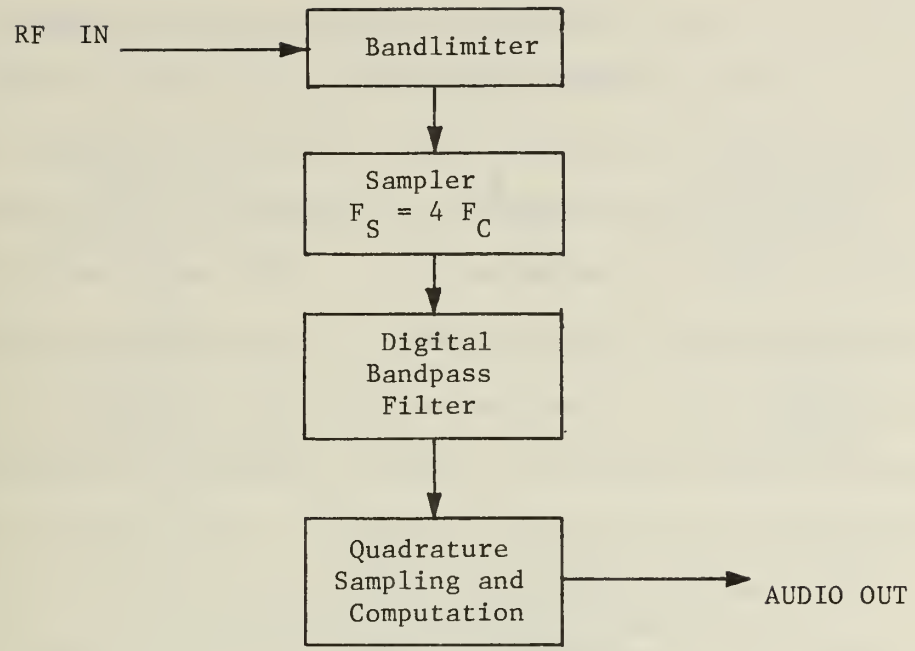
The two major steps of receiving an AM signal are:

1. Extraction of the desired signal from its environment (noise other signals, etc.).
2. Peak detection of this signal.

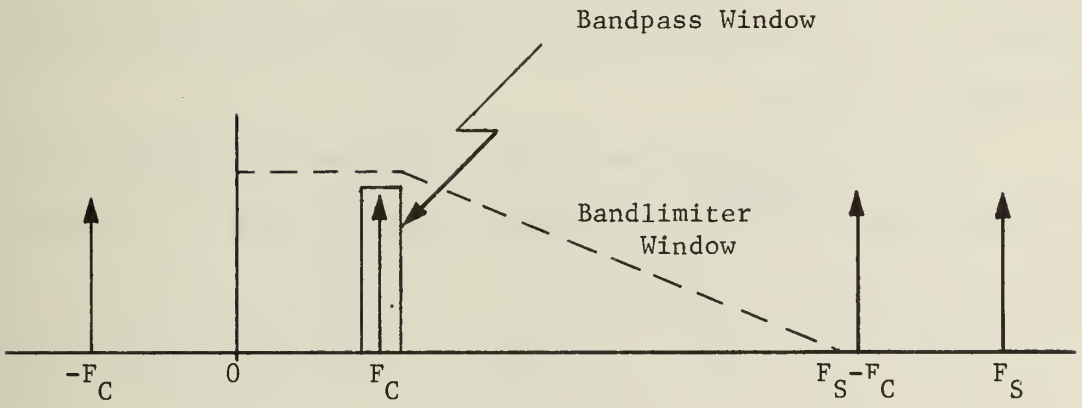
Two possible methods of performing these steps using quadrature sampling will be mentioned here.

One approach is to use a digital bandpass filter to extract the desired station, and then peak detect it by quadrature sampling the output of the bandpass. This is shown in Figure 3.1a. To avoid aliasing, the RF input must at least be sampled at $2F_C$. However to allow the quadrature sampler to be able to pick samples 90 degrees apart, and to ease the specifications on the bandlimiter, a sampling rate of $4F_C$ is required. Figure 3.1b shows this relationship along with the bandlimiting and digital bandpass spectra.

While the sample rate into the digital bandpass is F_S, the sample rate out of the quadrature sampler is much lower. Therefore the sample rate out of the digital bandpass filter may be much lower. However, since a bandpass rather than a lowpass is being considered, this is not true decimation. It would, however, allow a decrease in either system hardware or computational time.



(a)



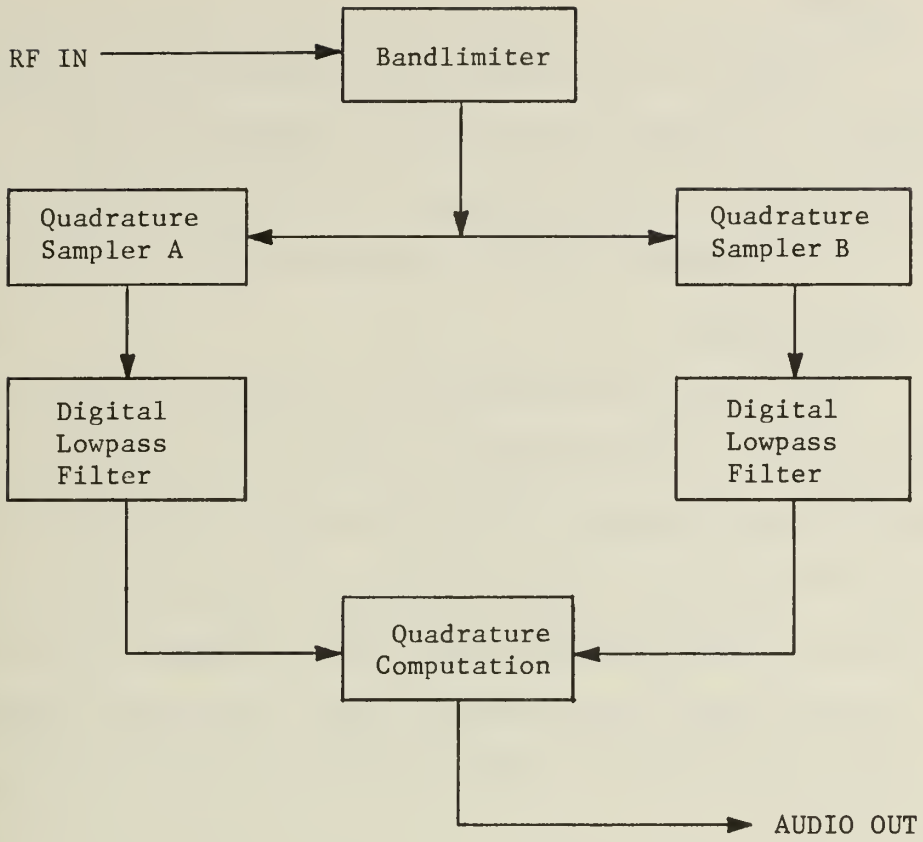
(b)

Figure 3.1 A Possible Receiver

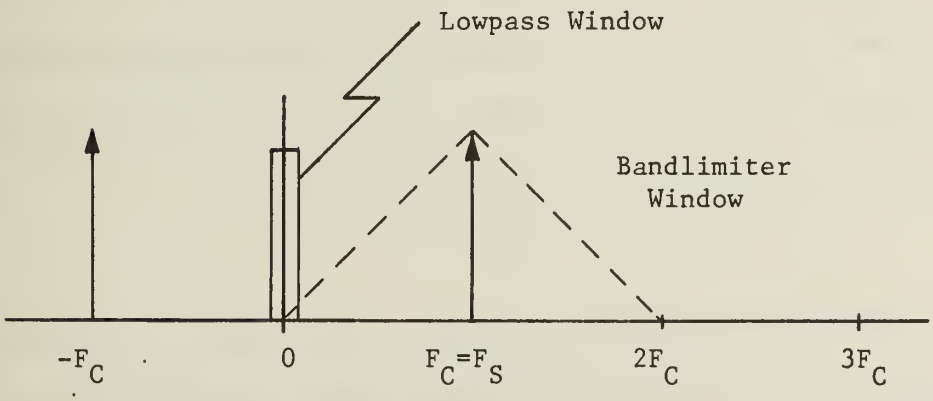
A second approach is to take advantage of aliasing to frequency shift the desired signal down to 0 Hz. In order to allow quadrature sampling, two samples, A and B, are taken every period of the desired carrier. The B sample is always taken one quarter of the period, or 90 degrees, after the A sample. Therefore, A and B samples are each taken at the frequency of the carrier with B samples in quadrature with A. Since each sampling fequency (F_S) is the same as the carrier frequency (F_C), both sample streams will alias the carrier down to 0 Hz. Since any multiple of F_C, as well as 0 Hz, will also appear as 0 Hz in the discrete time spectrum, they must be rejected as before with a bandlimiting circuit before the sampler. This is shown in Figure 3.2b.

Since the desired station now appears as a DC level in the two sample streams, we may now digitally lowpass filter the streams to extract this level. Notice that since the sampling rate in the A and B streams is F_C, the lowpass filter need only cycle at F_C, or one quarter as fast as the bandpass filter described above. Also note that since the quadrature sampler needs inputs only at an audio rate, the output sample rate of the lowpass filters may be lower than their input sample rates. This would allow decimation to be used in the filters, and therefore FIR implementations for these are preferred.

A block diagram for this type of receiver is shown in Figure 3.2a. The digital lowpass filters are assumed to decimate by M. The sampling rates are shown above the data paths.



(a)



(b)

Figure 3.2 An Alternative Receiver

4. INDIRAD

INDIRAD is a prototype built to demonstrate that quadrature sampling and Indicator processing can be used in a digital AM receiver. Being a demonstration unit, an effort was made to keep the hardware costs and complexity to a minimum while still demonstrating the principals involved.

4.1 Design Choices

Due to the lower sampling rates and use of lowpass rather than bandpass filters, the architecture of Figure 3.2 was chosen for INDIRAD. Since Indicator processing is most advantageous in very high speed applications. it was decided that the receiver should be designed to receive the highest frequencies which the hardware could handle. Indicator would be used in speed critical areas, while weighted binary would be used elsewhere. For the fastest possible speed, 10000 series ECL was chosen as the logic family to use.

Since the sampling rate of the output of the low pass filter is slower than that of its input, decimation can occur in the filter. As stated above, this implies the use of a FIR realization for the lowpass filters. Many excellent FIR lowpass filters can be designed using windows such as Hamming, Hanning and Blackman. Filtering is done by convolution of the input with the filter coefficients using:

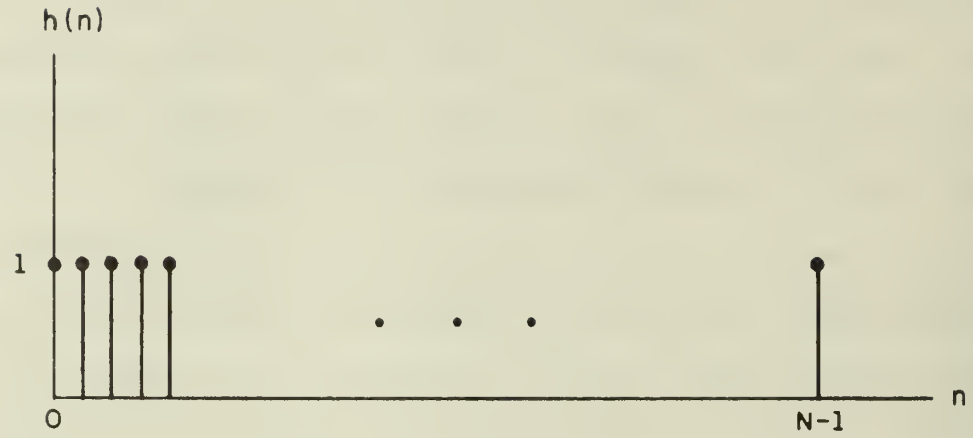
$$y(n) = \sum_{i=1}^{N} x(i)\, h(n-i)$$

where h(n) are the N filter coefficients. The difficulty with the filters mentioned above is that their coefficients must be represented to several significant digits. In addition, the product of the inputs and coefficients must also be represented to the same accuracy. However a two decimal digit coefficient would require a 100 bit Indicator number to represent it. This

would require more hardware than is justifiable with Indicator representation. Since the goal was not to build superior filters, it was decided to reject these complex filters for INDIRAD, and instead to use a simple rectangular window lowpass filter (Figure 4.1a). In this filter, all the coefficients have a value of one, and therefore multiplication is avoided.

When decimation by M is incorporated into an Nth order FIR filter, a significant hardware savings can be realized if M is greater than or equal to N. This results from the fact that any one filter input affects at most one output. Therefore after an input is multiplied by the appropriate coefficients and added into the summation, it may be discarded. The past N inputs need not be retained; only the value of the summation. For the rectangular window selected for INDIRAD, this could reduce the lowpass filters to summation blocks which would simply add N inputs together. Before adopting this simplification, a look at the effect on the input and output spectra is necessary.

It is well known that the magnitude of the spectra for a rectangular window is of the form SIN X/X. The lowest frequency zero of this spectrum is at F_S/N, the sampling frequency divided by the window width. Two double sideband AM stations must be seperated by at least $2F_A$, or twice the highest frequency of the audio modulating signal. Assume N is adjusted to place the lowest zero of SIN X/X at $2F_A$, where the closest stations might be. If the decimation ratio M equals N, then the output sampling rate of the filter will also be $2F_A$. Since this is exactly the Nyquist rate, aliasing will be avoided. Therefore decimation by N can be used to reduce the hardware without degrading signal quality. This decimation by N is used in INDIRAD.



a. $N = 2^i$

b. $N = 2^i$

Figure 4.1 Rectangular and Bi-Rectangular Filter Windows

In order to add N input samples together, the lowpass filters need to cycle only once per input. The single cycle will add the input to the summation. Since very little hardware is required to do this, another attempt should now be made to improve upon the frequency response of the lowpass filters.

The minimum stopband attenuation for a rectangular window filter is -13.25 dB. This can be improved by tapering the sides of the window, which is how the windows mentioned before are derived. In order to allow the window to be tapered, a filter coefficient other than 1 is necessary. A coefficient of 2 could be achieved in INDIRAD by cycling the digital lowpass filters twice on certain inputs. In order to determine the filter coefficients, using only 1's and 2's, which would give the best filter response, a fast fourier transform program was run on the computer. The best window which resulted is called a "bi-rectangular" window, and is shown in Figure 4.1b. This window has a minimum stopband attenuation of -19.7 db. The frequency spectrum is shown in Figure 4.2. Since this window requires cycling the filter twice during one input sample, it can only be used during the reception of signals that are less than half the maximum frequency of the receiver. On INDIRAD either the rectangular or the bi-rectangular filter window can be selected from a switch on the front panel.

4.2 The Hardware

A block diagram of INDIRAD is shown in Figure 4.3. Detailed logic drawings are given in the Appendix. While the general architecture could be drawn after the design choices of section 4.1 were made, the number of bits to be used for each data path still had to be determined. Since the precision used for each data path affects the overall signal to noise (S/N) ratio in a very complex manner, the radio was simulated on the computer. This

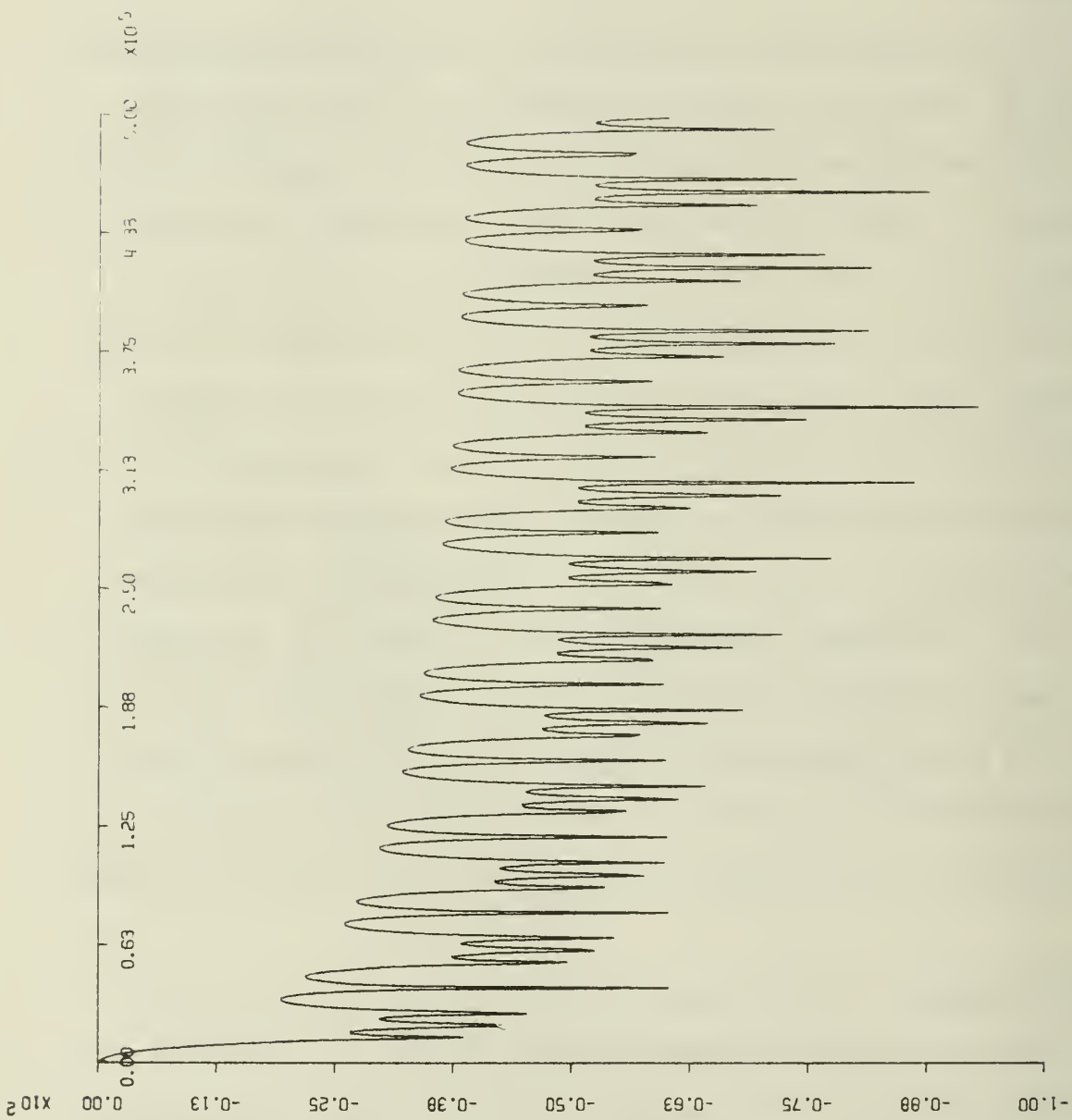


Figure 4.2 Spectrum for Bi-Rectangular Window

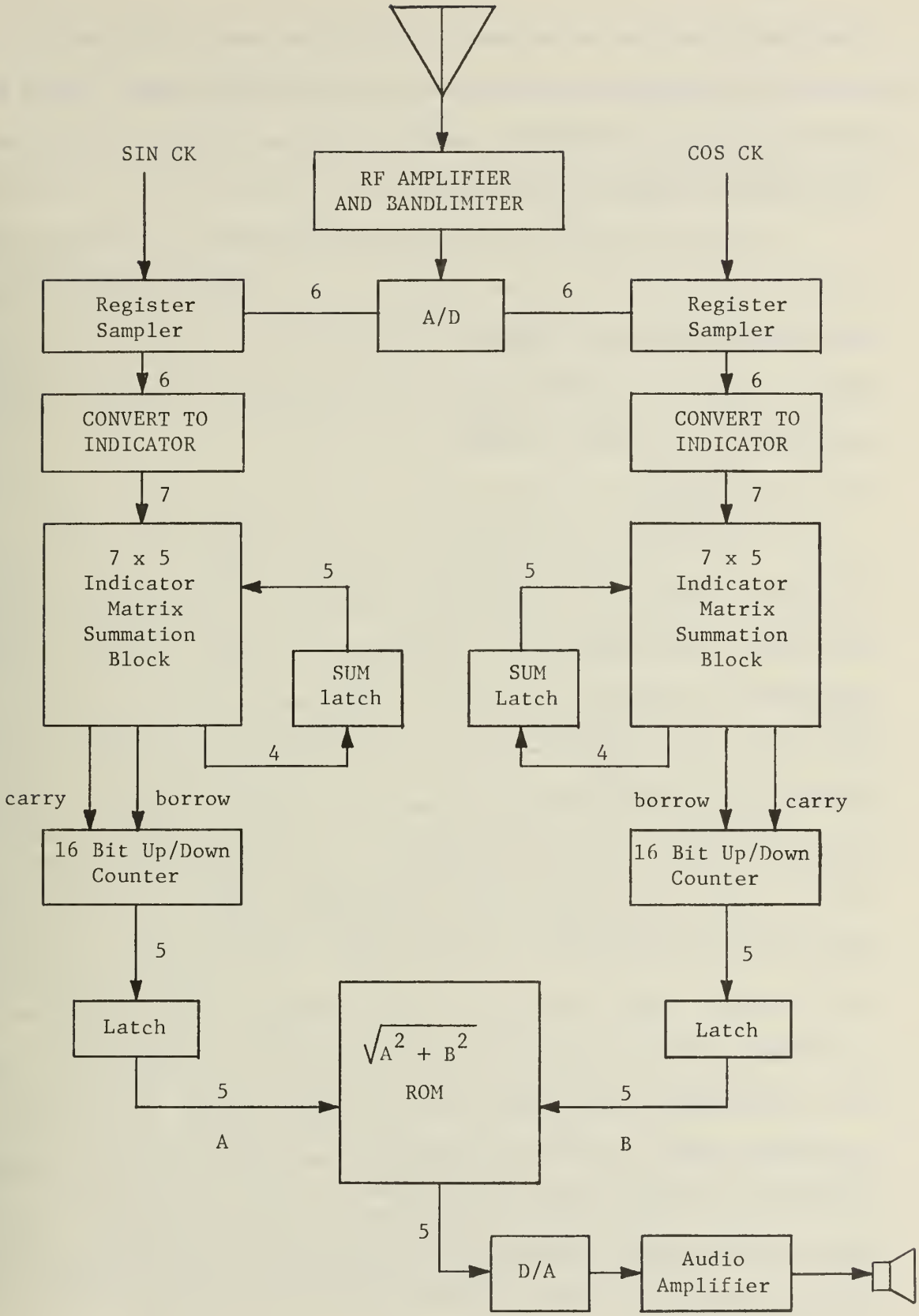


Figure 4.3 Block Diagram for INDIRAD

simulation program is interactive, allowing the user to vary any design parameter to determine its effect on the overall performance. Using this program, the number of bits for each data path was chosen such that no one path limits the signal to noise ratio.

One fact was notice while using the simulator. Varying a parameter may affect the S/N ratio of the receiver in an unexpected way (for instance, decreasing the RF gain may improve the S/N ratio by allowing a larger audio scale). Therefore as many parameters as possible are controlled from the front panel for the user to adjust.

4.2.1 RF to Digital

The RF signal from the antenna is first amplified before further processing. The gain of this amplifier (RF GAIN) is adjustable from the front panel. The signal is then bandlimited to remove any audio frequency components. To bandlimit the input as described in section 3.4 would require a tuned LC circuit, adjustable over the full range of the receiver (.5 to 50 MHz) Since the likelihood of finding a station at exactly a multiple of the tuned frequency is small, the simple highpass RC filter was deemed adequate.

The analog signal is then converted to a digital from using comparators as described in section 2.3. The comparators used were ECL differential line receivers. These work very well as comparators when input voltages are kept between -.25 volts and -3.0 volts. There are six comparators in the active quantization range, giving seven possible levels. An additional comparator at each end of the quantization range detects when the analog input exceeds the range of the A/D converters. This is indicated on the front panel as RF overflow. RF GAIN should be adjusted as high as possible without getting RF overflow.

This six bit unary number is then quadrature sampled by registers clocked with SIN CK and COS CK. As in section 3.4, these clocks are separated by degrees and are each at the frequency of the desired carrier. The six bit unary samples are then converted, by pairwise exclusive ORing, to seven bit Indicator numbers for further processing.

4.2.2 The Lowpass Filters

To receive an F_C = 50 MHz station having F_A = 5 KHz bandwidth, a rectangular window filter must sum $F_C/2F_A$ = 5000 samples to reject all other stations. Clearly a 5000 bit Indicator number is impractical. Examining the process of adding a 3 bit binary (7 level Indicator) number to a 13 or more bit (5000 level) sum reveals that full addition is required only for the lower 3 bits (7 levels). Therefore the addition of a filter input in INDIRAD is performed in two steps. The input, considered as a number from -3 to 3, is first added to the lowest order part of the sum, represented as an Indicator number in the range -2 to 2, by an Indicator matrix. The matrix outputs are a carry, weight 3, a borrow, weight -3, and the low order part of the sum, for the next itteration. The carry and borrow, of which only one can be active, then act as count up and count down controls for a 16 bit up/down binary counter. After adding N samples, the most significant portion of the sum lies in this counter.

A problem exists with the above circuit if an illegal Indicator value is introduced into the system. Such a value may be generated by the A/D converter or may appear in a register on power up. With a normal Indicator matrix being used for the adder, if an illegal value is introduced as an input, an illegal value will be generated as an output. Since this output is used as an input for the next itteration, illegal values will persist. In order to correct this, the sum latches in Figure 4.3 are 4 bit rather than 5 bit latches. The omitted value, the zero level, is generated from the latch

output only if no other output is on. This can be shown to correct for any illegal values introduced into this particular circuit within about three clock cycles. This also acts as a self resetting circuit on power up.

After summing N Inputs, N being determined from the front panel as 16 (NUMSPS + 2), the five most significant bits of the sum may lie in different places in the counter. These most significant bits must be selected in order to get the maximum signal out of the filter. To accomplish this, after the N samples have been added together, the counter is shifted right 16 times by parallel loading each bit from the next lower bit. After a certain number of shifts, a register will latch the high order bits of the counter. This number of shifts, which is entered from the front panel as SCALE, should be such that the most significant bits of the sum lie in the most significant bits of the counter when they are latched into the register. This register is thus the output of the filter. During right shifting, zeroes are shifted in from the left so that, after 16 shifts, the counter has been cleared.

4.2.3 Filters to Audio Output

The outputs, A and B, of the two lowpass filters are the quadrature samples that are required to compute the signal amplitude by the formula:

$$\text{Amplitude} = A^2 + B^2$$

This is done by table lookup in a Read-Only-Memory. A and B, each a 5 bit binary number, are combined to form a 10 bit number used as the address for the ROM. The content of this address is the value of the amplitude. This amplitude is then sent through a D/A converter, amplified, and sent to the speaker.

4.3 Performance of the Receiver

During simulation of the receiver, the model used for the RF world consisted of a variety of stations of equal signal strength and at various frequencies. The simulation showed that the receiver should show a S/N ratio of approximately 25 dB when tuned to any of these stations. In the local area where the actual receiver was built, there is one station many times more powerful than any other. This station comes in very clearly but is usually the only one receivable. On some days, usually in the morning, as many as four other stations can be received clearly.

The Indicator matrix has been measured to cycle in about 10 nanoseconds. This would support receiving stations up to 100 MHz. The 16 bit counters, however, can only cycle at about 50 MHz. This limits the upper frequency of the receiver.

During receiption of a station, a beat frequency is heard. This is a residual which is not cancelled out because of the limited precision of the data paths. To demonstrate that the quadrature sampling is removing most of the beat frequency, a switch on the front panel of INDIRAD will disable the output of one lowpass filter. When the quadrature sampler is thus defeated, the beat frequency becomes much louder.

5. Conclusions

In summary, the purpose of INDIRAD was to show that Indicator processing and quadrature sampling could be used in a digital AM receiver. This has been clearly demonstrated. An assessment of the applicability of these two concepts to future work will conclude this paper.

Indicator processing was shown to be faster than conventional weighted binary processing. The cost of this speed is additional hardware. Beyond about 4 binary bits, or 16 Indicator bits, the modest increase in speed does not justify the much greater increase in hardware. However, if there is a need for low precision high speed processing, Indicator processing should be considered.

Quadrature sampling is thought to be an excellent method of AM demodulation. A receiver consisting of an analog amplifier/bandlimiter, a high order digital filter with 12 to 16 bit precision, and a quadrature sampler is thought to be able to achieve a S/N ratio exceeding 80 dB. Such a receiver would be a superior product in any market place.

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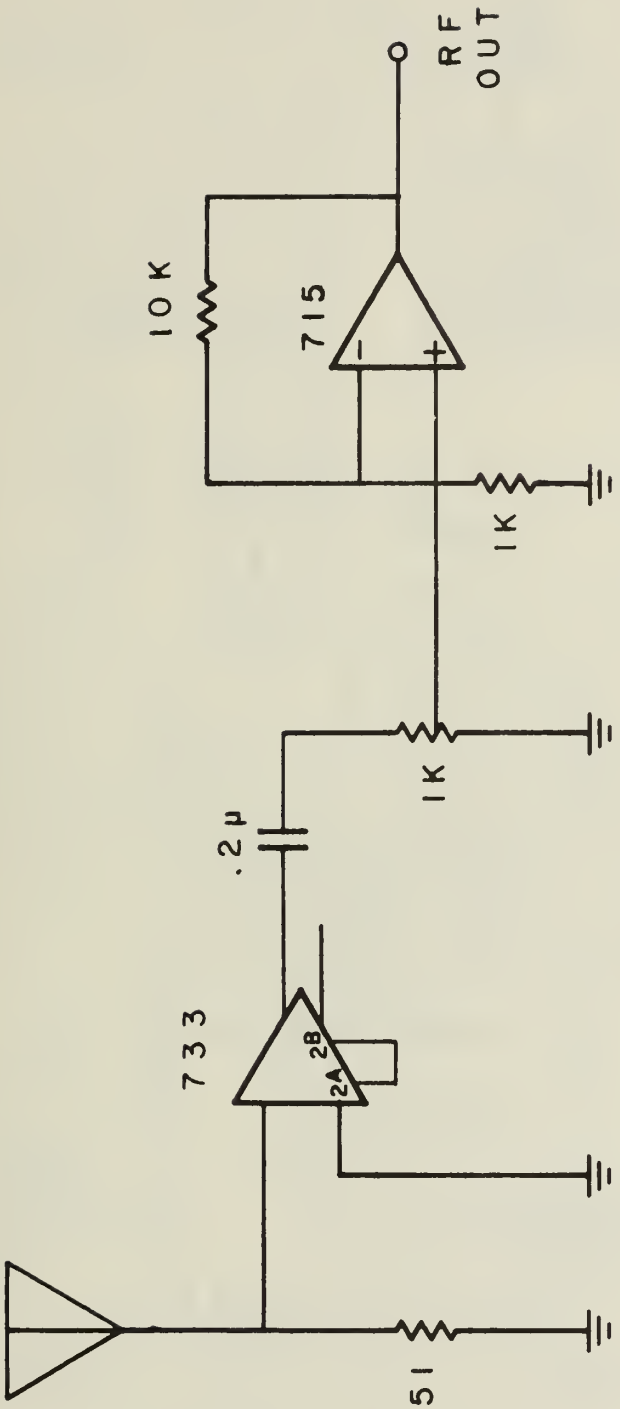
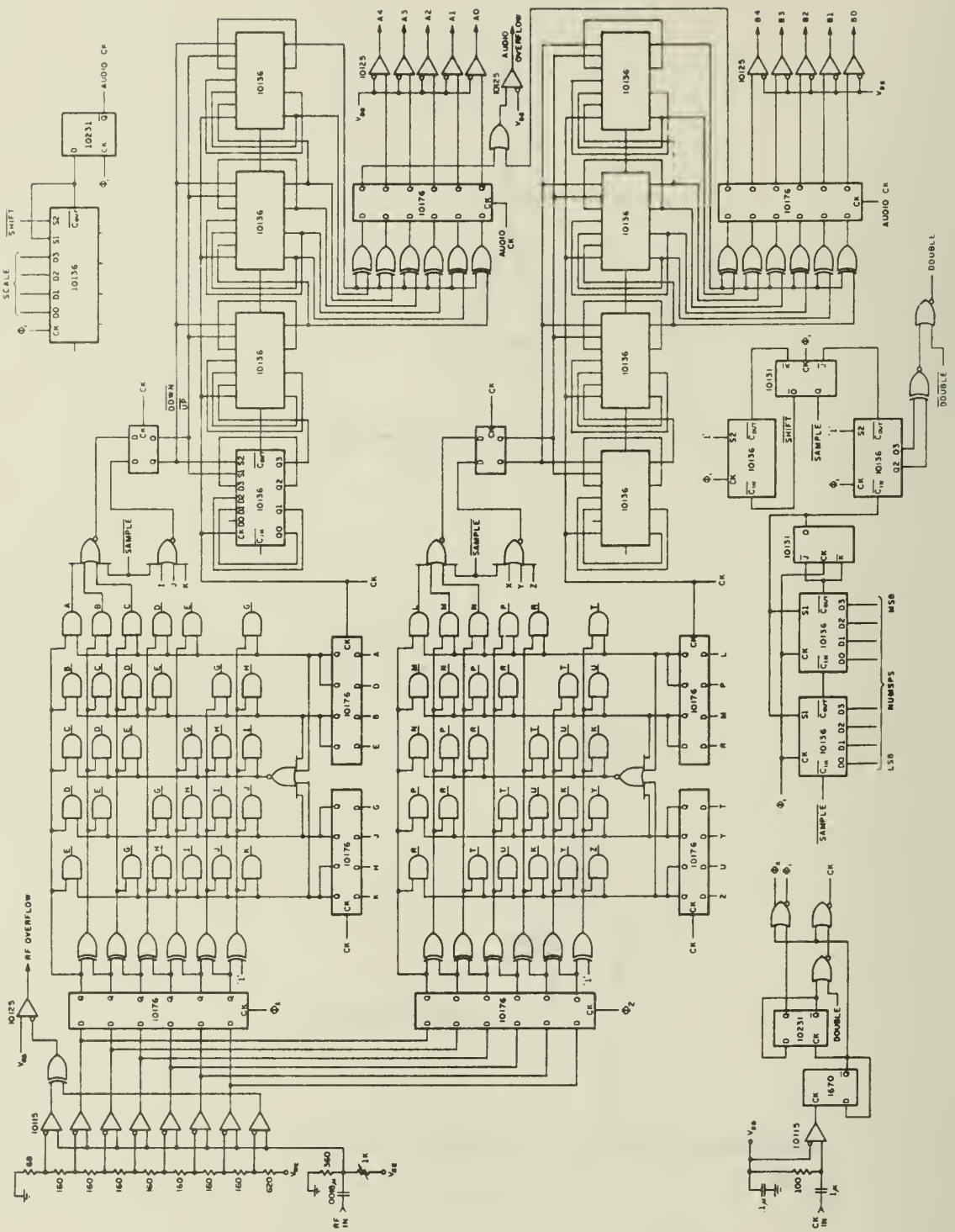
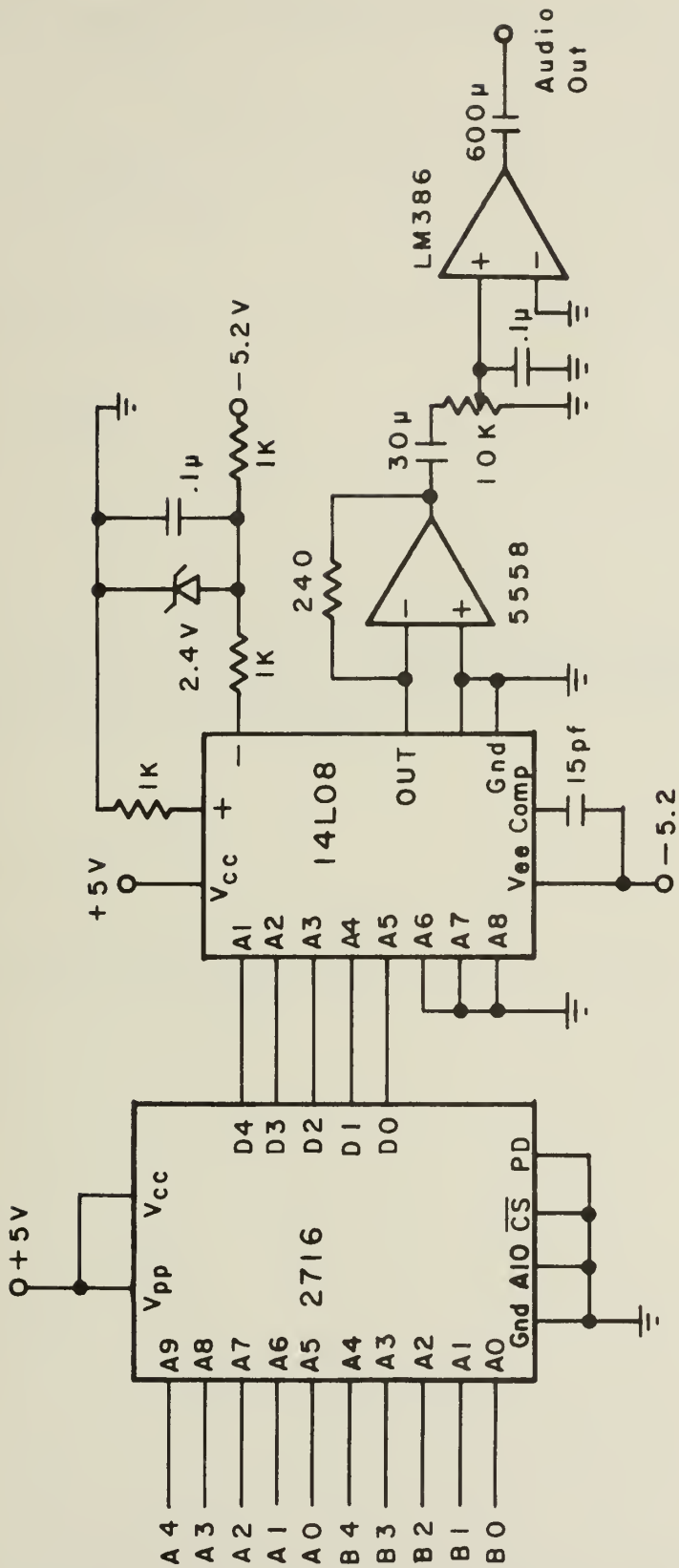
Appendix



RF Board



ECL Board


A4
A3
A2
A1
A0
B4
B3
B2
B1
B0
+5V
Vpp
Vcc
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
2716
D4
D3
D2
D1
D0
Gnd
A10
CS
PD
+5V
Vcc
A1
A2
A3
A4
A5
A6
A7
A8
14L08
OUT
Gnd
Vee
Comp
15pf
-5.2
1K
2.4V
1K
.1μ
-5.2V
1K
240
30μ
5558
10K
.1μ
LM386
600μ
Audio
Out

Audio Board

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16. Abstracts

The purpose of this reserach was to invetigate the application of indicator processing and quadrature sampling to the reception of broadcasted signals. The results of this study were used to build INDIRAD, a true digital receiver for amplitude modulated signals.

17. Key Words and Document Analysis. 17a. Descriptors

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digital reciver

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

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